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THESIS

LOW VOLTAGE OPERATIONAL AMPLIFIER USING
PARASITIC BIPOLAR TRANSISTORS IN CMOS

by

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June 1995

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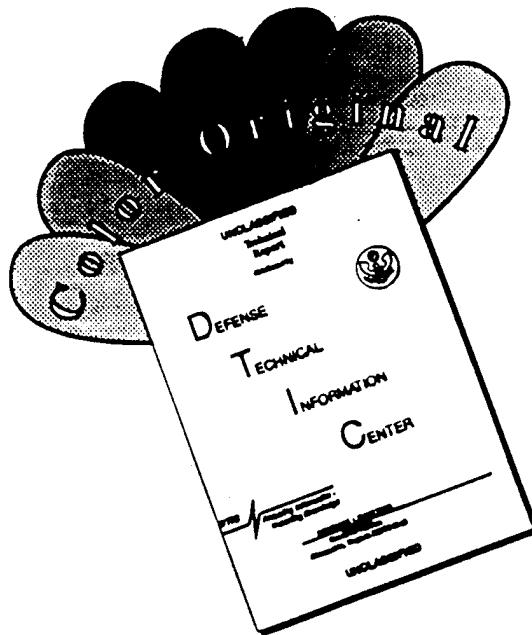
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LOW VOLTAGE OPERATIONAL AMPLIFIER
USING PARASITIC BIPOLAR TRANSISTORS IN CMOS

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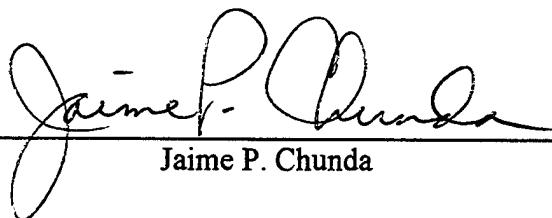
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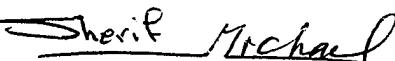
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ABSTRACT

In this research, a low voltage BiCMOS operational amplifier was built using parasitic bipolar transistors in bulk CMOS technology. Designed and analyzed using PSPICE circuit simulation software, the amplifier achieves a gain bandwidth product of 20.24 MHz with power supply voltages of $\pm$ 2.5 V. The simulation proved that the BiCMOS amplifier will operate with power supplies as low as $\pm$ 0.6 V. Using MAGIC VLSI software, a layout of the amplifier was made for eventual fabrication in the MOSIS 2.0 m CMOS process.

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I. INTRODUCTION

A. OVERVIEW

A fast, low power integrated circuit available at a low cost is always desirable. With portable battery operated devices becoming commonplace, the demand for circuits with these characteristics will only grow. Currently, low cost and low power can only be attained with standard CMOS technology. However, CMOS transistors have limited speed, current driving capability and noise performance. These limitations can be lessened with the incorporation of bipolar junction transistors (BJT) to the standard CMOS process to build BiCMOS type circuits.

Most existing BiCMOS processes combine high performance vertical BJTs with MOSFETs. These processes are expensive because of the extra steps needed to fabricate the buried layers for a good vertical BJT. Only devices whose use can justify this immense expense will be fabricated by this process. However, inexpensive parasitic lateral and vertical BJTs are available in any CMOS process without any additional processing steps. The vertical parasitic BJT is limited to common collector configurations because its collector is always tied to the substrate. The parasitic lateral BJT has low current gain, low current driving capabilities and a large base transit time since the minimum base width is limited by lithography. However, with the continual improvement of CMOS fabrication techniques to allow for more compact circuits, a small base width required for a useful lateral BJT can be made.

The operational amplifier is the most useful analog device. Analog to digital converters are among the many analog/digital systems that can benefit from an operational amplifier that is built with a BiCMOS configuration rather than just CMOS alone. One can expect an operational amplifier with a better signal to noise ratio and gain bandwidth product.

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This thesis proposes to build upon a previous amplifier designed by Holman and Connelly that used parasitic lateral bipolar transistors in the standard CMOS process [Ref. 1]. Improvements to this pseudo-BiCMOS amplifier were made to increase its stability in the closed loop configuration. The cost of this stability is a significantly reduced gain bandwidth compared to the base design. However, since the operational amplifier is predominately used in negative feedback circuits, the exchange of stability for gain bandwidth is limited if the operational amplifier is to be practically useful. This design uses the minimum phase margin as the measure for a useful operational amplifier.

This design will also illustrate how the parasitic lateral bipolar transistors can be used to build an amplifier that will operate effectively with low voltage power supplies. The simulation will show that the amplifier will have limited operation with a power supply of $\pm$ 0.6 V. The amplifier's operation with a power supply of $\pm$ 2.5 V was explored extensively through simulation.

B.   THESIS ORGANIZATION

The goal of this thesis was to build an operational amplifier that uses the parasitic bipolars in the CMOS process. The operational amplifier will be realized through Very Large Scale Integration (VLSI) implementation. The second chapter discusses CMOS technology and how CMOS transistors can be configured to operate as amplifiers. The next chapter introduces the bipolar transistor and its use in amplifiers. The operation and difficulties of using the parasitic lateral bipolar transistor in CMOS technology is explored. A comparison of the strengths and weaknesses of a CMOS transistor to a bipolar transistor is made. Chapter IV highlights the operational amplifier and considerations that must be made in its design. The pseudo-BiCMOS operational amplifier design is the topic of the fifth chapter along with its MAGIC layout. Simulation and analysis of the operational amplifier design is presented in chapter VI. Developed conclusions can be found in the seventh chapter, along with recommendations for further research and applications.

Appendix A contains the PSPICE circuit simulation code. Appendix B has color graphics of MAGIC layouts for the emitter dot structure, the BiCMOS operational amplifier and the four amplifier pad ring.

II. CMOS TECHNOLOGY

A. WHAT IS CMOS?

CMOS refers to a complementary metal oxide silicon structure much like a sandwich made of conducting silicon, insulating oxide and metal. Today, the metal gate is replaced by a polycrystalline silicon, but the metal name still remains. This structure forms a transistor, a three terminal device that can be used as an amplifier or a switch. The gate, source and drain are the names of the three terminals of the MOS transistor. Its basic structure is illustrated in Figure 1. The term complementary is used because two types of MOS structures, n-MOS and p-MOS, can be manufactured on the same substrate and can be used to complement each other to make devices. This complementary structure is especially useful in the building of digital components.
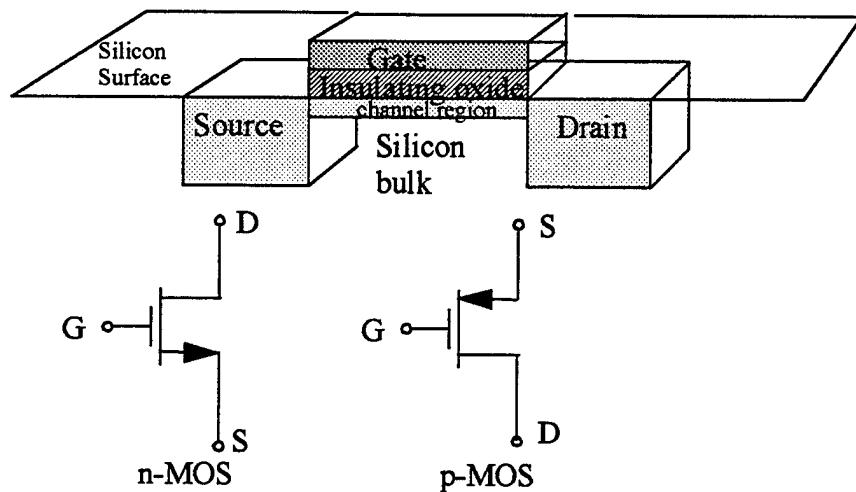
Figure 1: MOS transistor structure and symbols

B. CMOS CONSTRUCTION

The building block for most solid state devices is silicon. In its pure form, it is a semiconductor, having properties between those of a conductor and an insulator. Silicon is

the most dominant semiconductor material because it is cheap and plentiful, and its oxide (SiO_2) is an excellent electrical insulator.

If pure silicon is *doped* with certain impurities, it becomes a very effective conductor. Impurities that provide excess free electrons are called donor elements and produce an n-type silicon. Phosphorus, a pentavalent, is often used as a donor element. A p-type silicon is created when an impurity is added that provides *holes* or acceptors of free electrons. A trivalent element such as boron is used as an acceptor impurity.

1.   Silicon Wafer Processing

A single seed crystal of silicon is lowered into a vat of molten, doped, polycrystalline silicon and then extracted slowly to form an ingot. An ingot is a single crystal with a long cylindrical shape. Wafers are then cut from the ingot with an internal cutting-edge diamond blade. The wafer's width is between 0.25 mm and 1.0 mm thick. One of the wafer's sides is then polished. It is now ready for further processing into a semiconductor device. [Ref. 2 pp. 110-113]

2.   Further Doping to Create Devices

The creation of a semiconductor device requires selective placement of doping concentrations on the wafer. This is achieved with four different methods: epitaxy, deposition, ion-implantation and diffusion.

a.   *Epitaxy*

Epitaxy is the process of growing a single-crystal film on the wafer by subjecting the silicon wafer surface to a high temperature and the doping element.

b.   *Deposition*

Deposition requires the evaporation of the dopant element onto the wafer surface. This is followed by a thermal cycle, which drives the impurities into the silicon bulk.

c. *Ion Implantation*

Ion implantation subjects the silicon bulk to highly energized dopant atoms. The atom's energy drives it below the silicon surface to create a doped region.

d. *Diffusion*

High temperatures are used to diffuse the concentration of an impurity rich region to one of lesser content. The wafer is removed from the hot, impurity rich environment once the desired doping level is attained. It is important that the following process steps be at low temperatures or the intended doping may be altered.

Masks or special materials are used to mark the doped regions where desired. Photoresist, polysilicon, silicon dioxide (SiO_2), and silicon nitride (SiN) are some of the common masking materials used in the different processing steps.

Polysilicon used as the gate electrode also serves as a mask to define the source and drain electrodes. This is often referred to as a self-aligned process.

3. The Basic CMOS Process

There are two common CMOS technologies, the n-well process and the p-well process. The placing of an opposite doped well in the substrate allows for the presence of complementary n-channel and p-channel transistors on the same chip. The structure of an n-well process is illustrated in Figure 2.
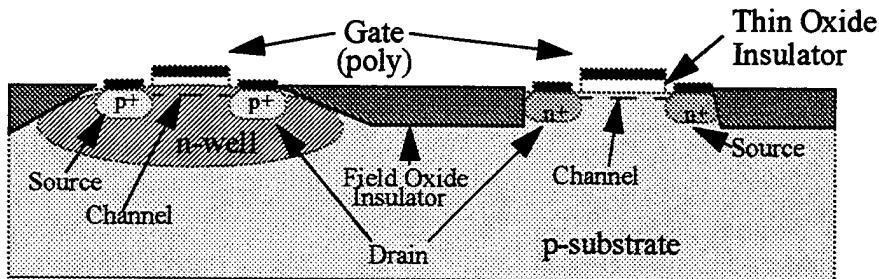
Figure 2: The CMOS n-well process

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C. MOS TRANSISTOR OPERATION

A positive voltage applied to the gate of a p-type substrate device will attract electrons to the region directly underneath the gate. If the gate voltage is positive enough, the accumulation of electrons would change the p-type material to an n-type material. This process forms an n-channel connecting the drain and the source so that a current can flow. The n-channel created by the gate voltage is a junction produced by an electric field. These types of transistors are often called field-effect transistors (FETs).

An n-FET will act like a voltage controlled switch that would be turned on when the gate to substrate voltage (V_{gs}) is greater or equal to the threshold voltage (V_T). A voltage between the drain and the source (V_{ds}) will conduct a current through the channel created by $V_{gs} \geq V_T$.

A positive voltage applied to the gate of an n-type substrate device will have the opposite effect. It turns the device off. A negative voltage applied to the gate will produce a p-channel created by the attraction of holes to the gate.

1. Basic dc Operation

MOS transistors have three regions of operation: cutoff, nonsaturation or linear, and saturation.

a. Cutoff region:

The MOS transistor is cutoff when

$$V_{gs} \leq V_T \text{ for n-MOS devices} \tag{Eq 2.1}$$

$$V_{gs} \geq V_T \text{ for p-MOS devices} \tag{Eq 2.2}$$

$$I_{ds} \approx 0 \tag{Eq 2.3}$$

b. Nonsaturation, linear, triode or ohmic region:

The nonsaturation region is present when

$$0 < V_{ds} < V_{gs} - V_T \text{ for n-MOS devices} \tag{Eq 2.4}$$

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$$V_{ds} \geq V_{gs} - V_T > 0 \text{ for p-MOS devices} \qquad \text{(Eq 2.5)}$$

The current between the drain and the source is given by the quadratic equation

$$I_{ds} = \beta \left[(V_{gs} - V_T) V_{ds} - \frac{V_{ds}^2}{2} \right] \qquad \text{(Eq 2.6)}$$

The region is linear when the term $\frac{V_{ds}^2}{2}$ is very small. [Ref. 2 pp. 51-52]

c. *Saturation region:*

The MOS transistor is saturated when

$$0 < V_{gs} - V_T < V_{ds} \text{ for n-MOS devices} \qquad \text{(Eq 2.7)}$$

$$0 < V_{ds} \leq V_{gs} - V_T \text{ for p-MOS devices} \qquad \text{(Eq 2.8)}$$

The saturation current is

$$I_{ds} = \beta \frac{(V_{gs} - V_T)^2}{2} \qquad \text{(Eq 2.9)}$$

The term β is the MOS transistor gain factor. It is dependent on both process parameters and device geometry, and is given by

$$\beta = \frac{\mu \varepsilon}{t_{ox}} \frac{W}{L} \qquad \text{(Eq 2.10)}$$

The device designer controls β by varying the W/L ratio where W is the width and L is the length of the transistor. The terms μ, ε and t_{ox} represent the effective surface mobility of the carriers in the channel, the permittivity of the gate insulator and the thickness of the gate insulator, respectively. These are dependent on process and are not alterable by the designer. [Ref. 2 pp. 51-52]

2. MOS Transistor As An Amplifier

Figure 3 shows a circuit that will use the MOS transistor to amplify the small signal v_{gs}. This small signal is superimposed upon the dc voltage V_{GS} that yields the total gate-to-source voltage V_{gs}, i.e.

$$V_{gs} = V_{GS} + v_{gs} \qquad \text{(Eq 2.11)}$$
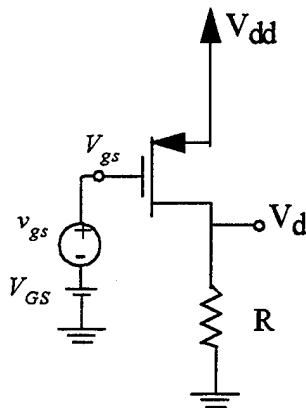
Figure 3: p-MOS transistor configured as an amplifier

The resistor R and the current through it will determine the value of V_{ds} by the relation

$$V_{ds} = V_{dd} - V_d = V_{dd} - I_d R \qquad \text{(Eq 2.12)}$$

The transistor should always be operated in the saturation region in order to perform as an amplifier. The current can then be expressed as

$$I_d = \beta \frac{(V_{GS} + v_{gs} - V_T)^2}{2} = \frac{\beta}{2}(V_{GS} - V_T)^2 + \beta(V_{GS} - V_T)v_{gs} + \frac{\beta}{2}v_{gs}^2 \qquad \text{(Eq 2.13)}$$

The term $\frac{\beta}{2}(V_{GS} - V_T)^2$ is recognizable as the dc or quiescent current, I_D. The last two terms on the far right of the equation are related to the input signal. One is directly proportional to the input while the other is proportional to the square of the input. This latter term represents nonlinear distortion and is not desirable. To minimize this distortion, the input signal must be kept small,

$$v_{gs} \ll 2(V_{GS} - V_T) \quad . \qquad \text{(Eq 2.14)}$$

If this is satisfied, we may neglect the last term and I_d becomes

$$I_d = I_D + i_d = I_D + \beta(V_{GS} - V_T)v_{gs} \qquad \text{(Eq 2.15)}$$

The constant relating the i_d and the input v_{gs} is the transconductance g_m ,

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$$g_m \equiv \frac{i_d}{v_{gs}} = \beta \left(V_{GS} - V_T \right) = \left. \frac{\partial I_d}{\partial v_{GS}} \right|_{v_{GS} = V_{GS}} \tag{Eq 2.16}$$

If one substitutes the definition of β given in the Eq. 2.10 into Eq. 2.16 above, g_m becomes

$$g_m = \left(\frac{\mu_p \varepsilon}{t_{ox}} \right) \left(\frac{W}{L} \right) \left(V_{GS} - V_T \right) \tag{Eq 2.17}$$

From this we see that transconductance depends on the W/L ratio of the MOS transistor. If a large g_m is desired, then the transistor must be wide but short. It is also dependent on the amount v_{gs} is greater than V_T. Transconductance is important because it is the parameter that measures the effectiveness of the transistor as an amplifier. Finally, from Eq 2.12, the voltage gain can be calculated

$$v_d = i_d R = g_m v_{gs} R \tag{Eq 2.18}$$

$$\frac{v_d}{v_{gs}} = g_m R \tag{Eq 2.19}$$

Thus, it can be seen that the transconductance is the transistor's effect on the amount of voltage gain realized. [Ref. 3 pp. 337-345]

III. BIPOLAR JUNCTION TRANSISTORS (BJTs)

A. WHAT IS A BIPOLAR JUNCTION TRANSISTOR?

Another common type of transistor is the bipolar junction transistor. It is called bipolar because both electrons and holes are involved in its operation. Its internal structure, resembling two back-to-back junction diodes, consists of two closely spaced pn junctions, that is, two dividing surfaces between semiconductor regions that are negative and positive relative to each other. Its three terminals are known as the emitter, the base and the collector. The central region of the transistor, the base, controls the current flowing between the outer emitter and collector regions. Current flow though the transistor when the emitter-base junction is "forward-biased"— that is, when a positive voltage applied to the base (npn transistor) attracts electrons from the emitter. The emitter's doping is such that there are many more electrons than there are holes in the base. The current flow is due to the electrons flowing into the base. Holes enter the base through the base terminal to neutralize the swept-in electrons to keep the emitter-base potential constant.

The base-collector junction is "reverse-biased". This means that the collector has a higher potential than the base. This sweeps the electrons from the base up to the collector. The base is made thin so electrons are less likely to be neutralized as they are swept up to the collector. This concept is illustrated in Figure 4.

Bipolar transistors are of two types, npn or pnp. The above discussion explains the active operation of an npn device. The pnp transistor's operation is somewhat reversed with the emitter-base junction being forward biased and the collector-base junction being reverse biased. The current flow is mostly due to holes, not electrons as in the case of the npn device.

B.   BJT OPERATION

There are three modes of BJT operation: cutoff, active and saturation modes. The cutoff and saturation modes are important if the transistor will be used as a switch. The active mode is useful when the transistor is used as an amplifier. This is the mode that was described briefly above.
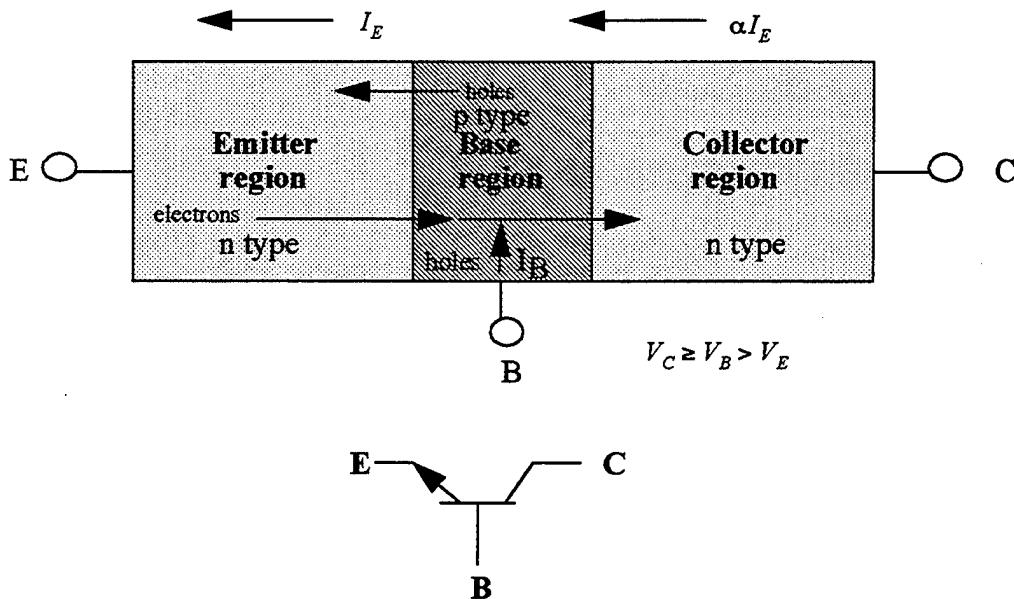
Figure 4: The bipolar transistor (npn)

1.   Cutoff and Saturation Modes

A BJT is "cutoff" when both emitter-base and collector-base junctions are reversed-biased. The current flow between the collector and the emitter is almost zero.

The saturation mode occurs when both emitter-base and collector-base junctions are forward-biased. The collector current acquires a linear relationship with the voltage potential between the collector and base regions.

2.   Active Mode Operation

Since we intend to use the BJT for its amplifying characteristics, more detail about the active operational mode will be given.

a.   The Collector Current

The collector current in the active mode has the approximate exponential relationship expressed as

$$I_C = I_s e^{(v_{BE})/V_T}$$ (Eq 3.1)

The term I_S is the saturation current, a constant current inversely proportional to the base width and directly proportional to the area of the emitter-base junction. V_T is the thermal voltage, approximately 25mV at standard room temperature. Notice that the active mode collector current is independent of collector voltage. [Ref. 3 p. 196]

b.   The Base Current

The base current is composed of two components. The most significant component is the one which is due to the holes being swept to the emitter because of the emitter's more negative potential. The second component is the holes that arrive through the base terminal to offset charge neutralization. Both components have an exponential relationship like I_C, so the base current can be expressed as a fraction of I_C as follows

$$I_B = I_C / \beta$$ (Eq 3.2)

$$I_B = (I_s/\beta) e^{V_{BE}/V_T}$$ (Eq 3.3)

β is referred to as the common-emitter gain and is used as a measure of the quality of a transistor. β is highly influenced by two factors: the base width and the relative dopings of the emitter and base regions. A high β is obtained through lightly doping a thin base and heavily doping the emitter. [Ref. 3 p. 196-197]

c. The Emitter Current

The emitter current is equal to the sum of I_C and I_B. Therefore, we may express it as follows:

$$I_E = I_C + I_B \qquad \text{(Eq 3.4)}$$

$$I_E = \frac{(\beta + 1)}{\beta} I_C \qquad \text{(Eq 3.5)}$$

We can now alternately express I_C in terms of I_E

$$I_C = \alpha I_E \qquad \text{(Eq 3.6)}$$

α can be expressed in terms of β by

$$\alpha = \frac{\beta}{\beta + 1} \qquad \text{(Eq 3.7)}$$

α is called the common-base gain and since β ranges from 100 to 1000, α is very close to unity. [Ref. 3 p. 197]

3. Equivalent Circuit Model

A first order model of an active mode BJT can be represented by the equivalent circuit in Figure 5. The diode between the base and the emitter has a current scale factor of I_S/β. The current-source is controlled by I_B, which is scaled by the β of the transistor. [Ref. 3 p. 198]
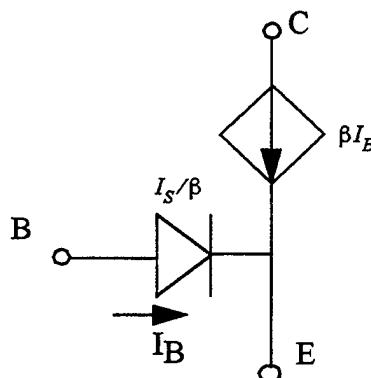
Figure 5: Large signal circuit model of BJT in active mode. [Ref. 3 p. 198]

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C. THE BJT AS AN AMPLIFIER

As stated before, the BJT must be in the active mode to be used as an amplifier. Figure 6 shows a circuit in which a BJT is configured to amplify the small signal v_{bc}.

The total emitter-base voltage becomes

$$V_{eb} = V_{EB} + v_{eb} \qquad \text{(Eq 3.8)}$$

The collector current is given by

$$I_c = I_S e^{(V_{EB} + v_{eb})/V_T} = I_S e^{(V_{EB}/V_T)} e^{(v_{eb}/V_T)} = I_C e^{v_{eb}/V_T} \qquad \text{(Eq 3.9)}$$

If the exponential is expanded in a series and ignoring the higher order terms for small signals, then the current can be expressed as

$$I_c = I_C\left(1 + \frac{v_{eb}}{V_T}\right) = I_C + \frac{I_C}{V_T}v_{eb} \qquad \text{(Eq 3.10)}$$

The total collector current has two components: the dc or quiescent current, and the small signal current. The small signal current is now related to the input voltage so the collector current can also be expressed as

$$I_c = g_m v_{bc} \qquad \text{(Eq 3.11)}$$
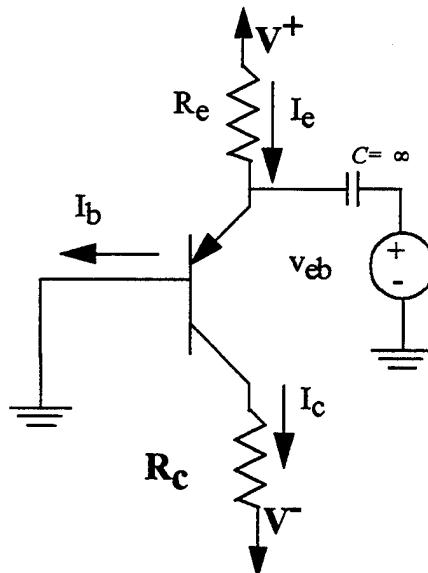
Figure 6: A pnp bipolar transistor configured as an amplifier.

The transconductance g_m is given

$$g_m = \frac{I_C}{V_T}.$$ (Eq 3.12)

The transconductance of a BJT is directly related to the quiescent collector current and not to the transistor's dimensions as in the case of the MOS transistor. This is valid as long as the input signal is small. [Ref. 3 pp. 220-222]

Finally, the voltage gain, G, of the BJT can be derived from the circuit in Figure 6

$$V_c = I_c R_c = (I_C + i_c) R_C = V_C + i_c R_c$$ (Eq 3.13)

$$v_c = i_c R_c = g_m v_{eb} R_c$$ (Eq 3.14)

$$G \equiv \frac{v_c}{v_{eb}} = g_m R_c \quad . \text{[Ref. 3 p. 225]}$$ (Eq 3.15)

D. COMPARISONS BETWEEN BIPOLAR AND MOS TRANSISTORS

Table 1 below lists the differences between bipolar and MOS transistors. It can be seen here that any design that can combine the two may eliminate the inherent weaknesses of a design based on only one transistor type.

	MOS	BJT
Advantages	high input impedance high current gain low input bias current	high transconductance high voltage gain low offset voltage low noise voltage wide range of collector currents
Disadvantages	low transconductance low voltage gain high offset and noise voltage small range of drain currents	low input impedance low current gain high input bias current

Table 1: Comparisons of MOS and bipolar transistors [Ref. 4 p. 152]

E. THE LATERAL PARASITIC BJT IN CMOS

1. Structure

The BJT that will be used in the design of this operational amplifier must be constructed using standard CMOS technology. The only type of BJT that can be realized without adding additional costly procedures to the fabrication process is the parasitic BJT that exists in any CMOS structure. The CMOS process chosen is n-well and p-substrate. Only pnp BJTs can be made from this process. This is shown in Figure 7.

2. Factors Limiting Performance

Notice that the emitter is square and surrounded by the collector and the base. This is necessary to collect as much of the emitted current as possible and to keep the injection around the emitter evenly distributed. The base width is denoted by d_l. This is determined by the smallest gate length that a CMOS process can deliver. The MOSIS process that will be used to manufacture this amplifier can deliver a gate length of 2 μm. Conventional BJTs have base widths ranging from 0.5-0.8. μm. Since the current gain β of a BJT is highly dependent upon the base width, we can expect that β of this device to be smaller than that of a conventional BJT. It is apparent that as CMOS technology improves to make gates smaller, it also improves the gain of these parasitic devices as well.

Figure 7 also shows that there are three possible BJTs, a lateral and two vertical. One vertical lies between the emitter and the p substrate and the other between the collector and the p substrate. The vertical one between the collector and the substrate is always cutoff and so can be ignored. The other is always on and always operates in parallel with the intended lateral one. This BJT is only useful in a common collector configuration. Hence, it is usually a parasite to the lateral one. A buried layer of n+ between the well and the substrate would lessen the effect of this parasitic transistor but not completely eliminate it. The process required for the placement of this n+ layer is beyond standard CMOS technology, so this parasitic transistor must be taken in account.

Another problem results from the shallow depth of the p-diffused regions which is used to make the CMOS source and drain, but here it is used to make the collector and the emitter. This shallow depth translates to a small emitter-base junction area which affects the saturation current.

The base current of the device has two components given by

$$i_B = (i_{Bl} + i_{Bv}) = i_{Bl}(1 + K_{vl}) \qquad \text{(Eq 3.16)}$$

$$K_{vl} = \frac{i_{Bv}}{i_{Bl}} = \frac{2A_{EBv}d_v}{A_{EBl}d_l} = \frac{d_E d_v}{2d_p d_l} \qquad \text{(Eq 3.17)}$$

The term K_{vl} is a reduction factor introduced to account for the parasitic transistor. The terms A_{EBv} and A_{EBl} are the injection area of the vertical and lateral transistor, respectively. The injection area of the lateral transistor is the perimeter of the emitter. d_p and d_E are the depth of the diffused p-layer in the n-well and the width of the emitter, respectively. [Ref. 5 p. 137]

Since this lateral BJT has a large base width, its base current is greatly affected by the increased chance of transiting charge recombination. If we think of the base current as the electrons entering to offset recombination, then another way to express base current is

$$i_{Bl} = \frac{Q_F}{\tau_{BF}} \qquad \text{(Eq 3.18)}$$

Q_F is the dynamic excess charge in the base and τ_{BF} is recombination time constant. The current gain β can then be expressed as a ratio of two time constants

$$\beta = \frac{\tau_{BF}}{\tau_F} \frac{1}{1 + K_{vl}} \qquad \text{(Eq 3.19)}$$

$$\tau_F = \frac{d_l^2}{2D_p} \qquad \text{(Eq 3.20)}$$
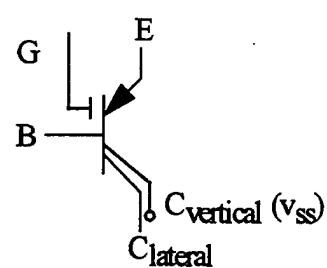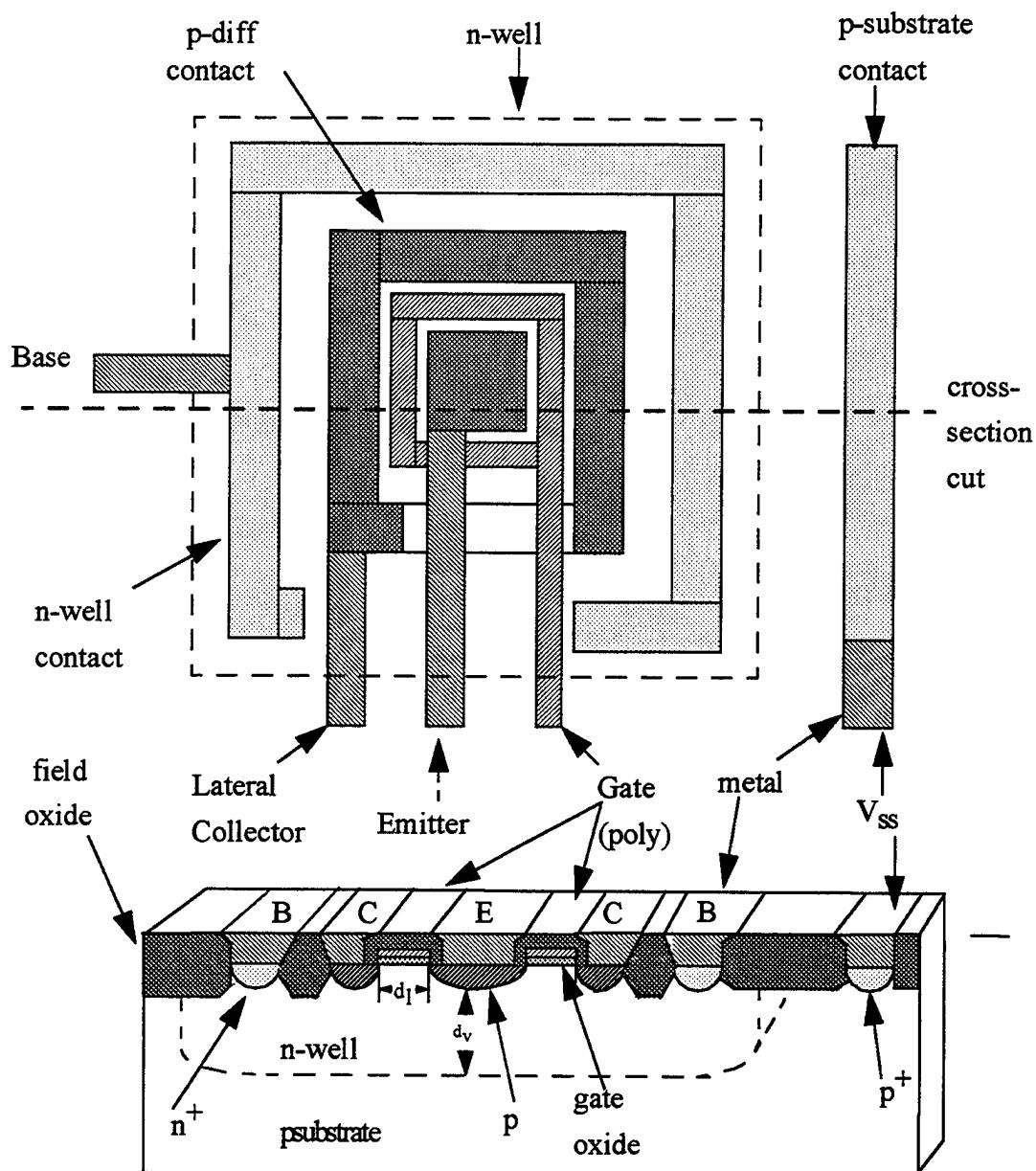
Figure 7: The layout of a single emitter dot lateral pnp bipolar transistor

The term τ_F is the base transit time which is the time for the holes to diffuse through the base. D_p is the diffusion constant for holes related to mobility by Einstein's relation and given by

$$D_p = \mu_p kT/q. \qquad \text{(Eq 3.21)}$$

where μ_p is the mobility of holes, k is Boltzman's constant, T is the temperature in degrees Kelvin and q is the charge of the electron. [Ref. 5 p. 137-138]

As seen from the above equations, greater value of β can be achieved by reducing the base width and minimizing K_{vl}. This would mean a deeper p-diffusion, shallower n-well and a smaller emitter length.

Figure 7 above, depicts the "emitter dot" structure, with a minimum emitter length, satisfying the above procedure to achieve large β.

The current gain β can also be maximized for this structure by limiting the emitter current. It has been determined that efficiency of the lateral BJT, with respect to the vertical, decreases as the emitter current increases. By limiting the emitter current to 5 μA for this emitter dot structure, a lateral efficiency of at least 70% is attained. If higher emitter currents are desired, a multi-emitter dot layout should be used instead of a single large emitter contact. [Ref. 1]

3. The CMOS Gate

The polysilicon gate must be biased properly so that the MOS transistor is turned off, allowing the BJT to operate. A small positive voltage of at least 250 mV applied to the gate will achieve this. Increasing the gate voltage to V_{dd} will improve low frequency noise performance by driving minority carriers in the base deeper into the n-well and away from surface defects. [Ref. 1]

IV. OPERATIONAL AMPLIFIERS

A. WHAT IS AN OPERATIONAL AMPLIFIER?

An operational amplifier (refered to as "op amp " for brevity) is an integrated circuit that is capable of sensing and amplifying dc and ac input signals. Originally, operational amplifiers were used for analog computing circuits, control circuits and instrumentation. Now they can be found virtually anywhere in audio reproduction, communication systems, digital processing systems and consumer electronics.

B. THE IDEAL OPERATIONAL AMPLIFIER

An ideal operational amplifier is a direct coupled device with two differential inputs and a single output. A positive signal at the non-inverting input, with respect to the inverting input, will produce a positive output. A positive signal at the inverting input, with respect to the non-inverting, will produce a negative output. The output voltage is A_{v0} times the input differential voltage V_{in}. A_{v0} is called the open-loop gain of the amplifier.

Ideally, an operational amplifier would have these characteristics:

1. The voltage gain is infinite: $A_{v0} = \infty$.

2. The input resistance is infinite: $r_{in} = \infty$.

3. The output resistance is zero: $r_o = 0$.

4. The bandwidth is infinite: $BW = \infty$.

5. There is zero input offset voltage: $V_o = 0$ if $V_{in} = 0$. [Ref. 6 p. 4]

An idealized amplifier is shown in Figure 8.

From the above, we can deduce two important properties of an ideal operational amplifier. Since its gain is infinite, any infinitesimal input voltage will produce an output, so differential input voltage is always zero.

Also, since input resistance is infinite, there is no current flow into either of the input terminals.
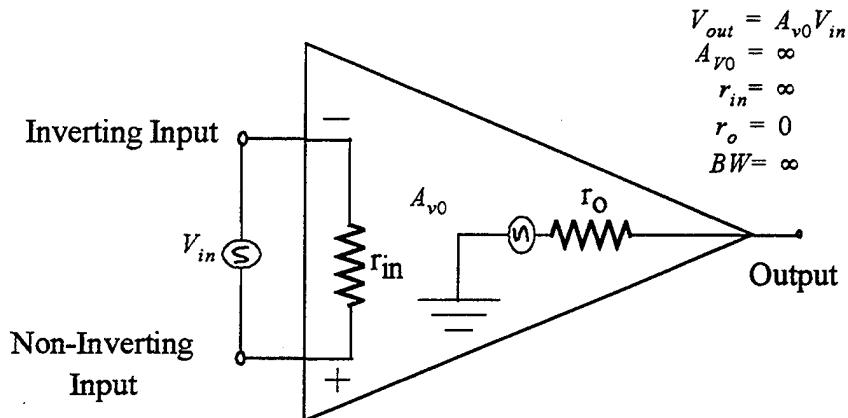

Figure 8: The Ideal Operational Amplifier [Ref. 6 p. 4]

C. THE NON-IDEAL OPERATIONAL AMPLIFIER

In the real world, the ideal operational amplifier does not exist. The measure of the quality of an actual operational amplifier is how close to the ideal will it perform.

1. Gain-bandwidth Product

Of course, there is no amplifier that can deliver infinite gain. Voltage gain can be large, but only at low frequencies. A non-ideal op amp will always deliver either gain or bandwidth at the expense of the other. The open loop gain of a typical op amp plotted against frequency usually has the shape of the curve of Figure 9. The constant slope of decreasing gain is necessary for stability in closed loop systems, in which op amps have the most application. The frequency where the gain of the op amp decreases to unity is called the unity-gain frequency. It is also known as the gain-bandwidth product and is given as

$$GBP = gain \times bandwidth_{3dB}$$

(Eq 4.1)

Gain-bandwidth product is the most important parameter for any op amp. The goal of many op amp designers is to achieve the highest product possible.
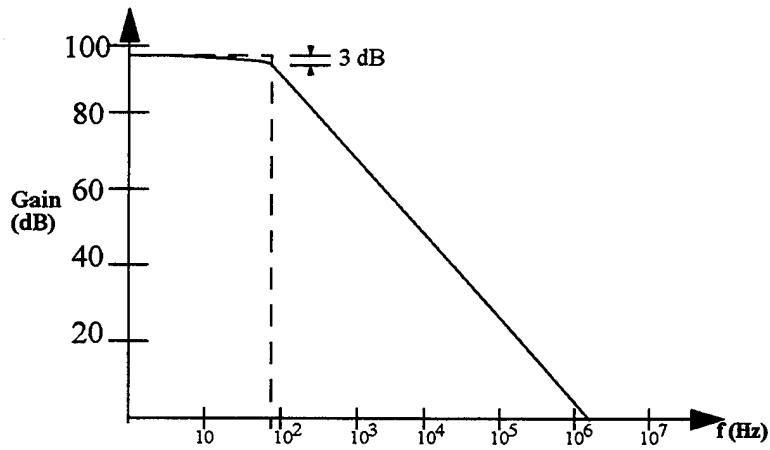

Figure 9: The gain of typical op amp

2.   Input and Output Impedance

An op amp designer would like to make the input impedance of his amplifier as close to infinity as possible. Actual op amps have an input impedance of 1 MΩ or more, while some have up to 100 MΩ. This is an area where the MOS transistor clearly has an advantage over the BJT because its input gate does not draw any current.

The output impedance should be near zero. Real devices have output impedances ranging from 25 Ω to 4000 Ω. [Ref. 7 p. 11]

These input and output impedances are important in closed loop applications as they directly impact the gain of the device. Generally, if the input impedance is at least ten times that of feedback source resistance and output resistance is no more than one tenth of load resistance, no problems will be encountered.

3.   Input Bias Current, Input Offset Current and Output-Offset Voltage

Ideally, there should be no current flowing into the inputs of an op amp. However, a real op amp requires a small input current to each of its two input terminals in order to

operate. The average input current of the two is called the input bias current. The current difference between the two is called the input offset current. In a closed loop system, the input bias current gives rise to an output-offset voltage, the bias current multiplied by the feedback series resistor. This offset voltage can be nearly nulled out by connecting a resistance in series with the positive input terminal equal to the total dc resistance seen by the negative input terminal. [Ref. 7 p. 11]

4. Input-Offset Voltage

The output voltage of an op amp should be zero when the differential voltage at the inputs is zero. However, there may be an output voltage due to the amplifier's high gain which amplifies any slight unbalance. The voltage applied to one of the terminals to bring the output voltage to zero is called the input offset voltage. [Ref. 7 p. 11]

5. Slew Rate

Slew rate is the maximum rate of change of an op amps' output voltage, expressed as

$$SR = \left.\frac{dv_o}{dt}\right|_{max}.$$ (Eq 4.2)

The slew rate is a large signal parameter. Large input signals that exceed an op amp's slew rate limitation will experience non-linear distortion. Slew rate limitation is due to the op amp's internal compensating capacitance. A higher slew rate equates to a wider frequency bandwidth. It is usually specified for the unity gain configuration in V/μs. [Ref. 3 pp. 86-87]

6. Common Mode Rejection Ratio

An amplifier should only amplify differences between the two input terminal voltages. However, every amplifier will generate some small gain due to a signal that is common to both inputs. Common mode rejection is the ability of an amplifier to resist this common mode gain. This ability is expressed as the common-mode rejection ratio, defined as

$$CMRR = \frac{|A|}{|A_{cm}|}.$$ (Eq 4.3)

It is expressed commonly in decibels as

$$CMRR = 20\log\frac{|A|}{|A_{cm}|}$$

(Eq 4.4)

The term A is the differential gain, while A_{cm} is the common mode gain. A higher ratio equates to a better rejection. The ratio is frequency dependent, decreasing as the frequency increases. Common values of CMRR range from 80 to 100 dB at low frequencies. [Ref. 3 pp. 90-91]

7.   Power Supply Rejection Ratio (PSRR)

The power supply rejection ratio is the sensitivity of an op amp to noise in the power supply. It is defined as

$$PSRR = \frac{A_v}{A_{dd}}$$

(Eq 4.5)

The term A_v represents the gain when there is no differential input to the power supply terminals of the op amp. A_{dd} is the gain that occurs when there is a differential input to the power supply terminals, while no differential input voltage is applied to the input nodes.

If an op amp is in a unity gain configuration with the non-inverting input grounded, the PSRR becomes

$$PSRR = \frac{V_{dd}}{V_{out}}$$

(Eq 4.6)

where V_{dd} is the differential input applied to the power supply node and V_{out} is the output voltage due to the differential input. [Ref. 8 p. 415]

D. THE OPERATIONAL AMPLIFIER DESIGN

Op amps usually have the basic architecture represented in Figure 10. The input stage of the op amp is the differential transconductance stage. This stage provides a good measure of the overall gain. It is primarily responsible for the noise performance and the offsets of the op amp. The high gain stage adds gain to what is already provided by the input stage. If the input stage does not transform a differential input to single-ended output, the

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high gain stage will make the conversion. If the load resistance the op amp will drive is low, a buffer stage would be needed to lower the output resistance in order to maintain a large signal swing. Compensation will be necessary for stable operation in the closed loop configuration. The bias circuit distributes a stabilized bias current to each of the previous stages. [Ref. 8 pp. 366-367]
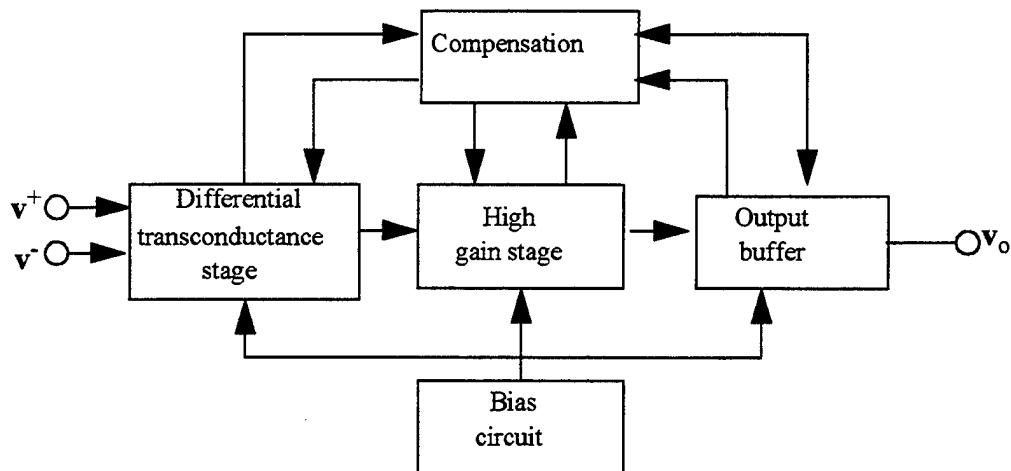

Figure 10: Basic op amp architecture [Ref. 8 p. 366]

1. **Differential Transconductance Stage**

This input stage usually consists of a source/emitter coupled differential pair with a current mirror load and a current sink or source for biasing. In the following sections each of these sub-circuits, will be examined.

a. The differential pair

The most useful analog sub-circuit, the differential pair, functions as the input to the op amp. The differential pair consists of two equal or matched transistors which are biased by a current source as in Figure 11. If v_i is zero, then the currents i_1 and i_2 will both

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equal $\frac{I}{2}$. If one recalls Eq. 3.1, each collector current may be expressed as

$$i_C = I_S e^{\left(\frac{v_{eb}}{V_T}\right)}$$ (Eq 4.7)

and that they both add to I, which may be expressed as

$$I = i_1 + i_2 = I_S \left[e^{\frac{v_{eb1}}{V_T}} + e^{\frac{v_{eb2}}{V_T}} \right]$$ (Eq 4.8)
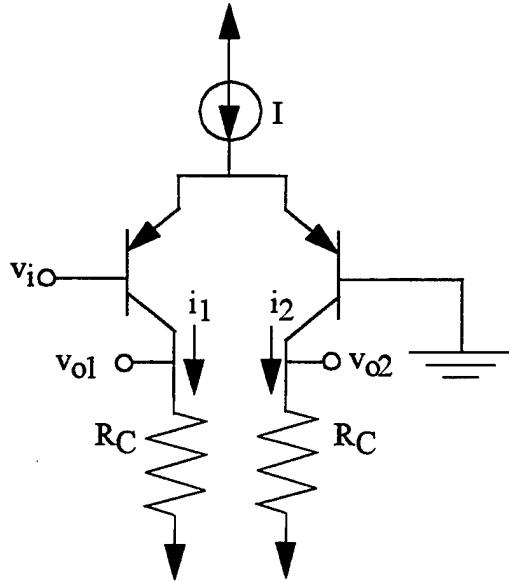
**Figure 11: The differential pair**

The output differential voltage is

$$v_{od} = v_{o1} + v_{o2} = R_C i_{od}$$ (Eq 4.9)

where

$$i_{od} = i_2 - i_1 = I_S \left[e^{\frac{v_{eb2}}{V_T}} - e^{\frac{v_{eb1}}{V_T}} \right].$$ (Eq 4.10)

Once v_i reaches a small value above zero, an input differential voltage will exist and will be

$$v_i = v_{eb1} - v_{eb2}$$ (Eq 4.11)

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The substitution of v_{eb1} from Eq. 4.11 into Eq. 4.8 and Eq. 4.10 allows it to be eliminated. The division of Eq. 4.10 by Eq. 4.8 also eliminates v_{eb2} and results in

$$\frac{i_{od}}{I} = \frac{e^{\frac{v_{id}}{V_T}} - 1}{e^{\frac{v_{id}}{V_T}} + 1} = \tanh\left(\frac{v_{id}}{2V_T}\right) \qquad \text{(Eq 4.12)}$$

This expression is displayed graphically in Figure 12, along with the similar expression for a MOS differential pair. The constant slope centered at the origin is the small signal gain. For $x < 1$, $\tanh x \approx x$ and

$$v_{od} = R_C I \frac{v_{id}}{2V_T} \qquad \text{(Eq 4.13)}$$
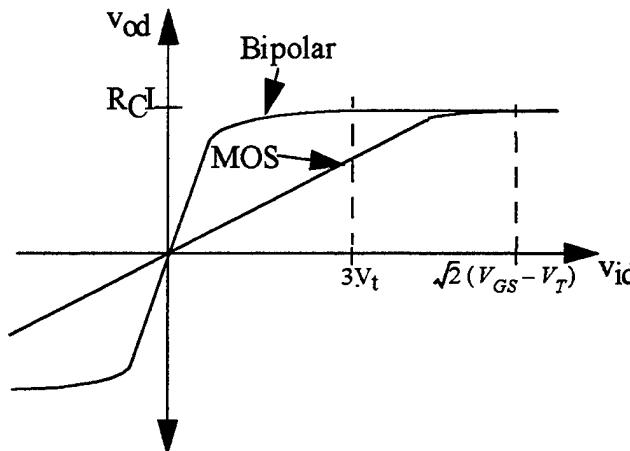
Figure 12: Small signal gain of the bipolar and MOS differential pairs [Ref. 5 p. 374]

The MOS differential pair has a much flatter gain. It can approach the bipolar's gain if $V_{GS} - V_T$ is small, but this is only obtainable at low currents.

Input referred noise is another important consideration. The bipolar transistor gives better noise performance than the MOS transistor. Of both types of MOS transistors, the p-MOS gives better noise performance than n-MOS by a factor of five [Ref. 8].

The input impedance of the MOS transistor is practically infinite. Bipolars have a finite resistance due to the base input biasing current. If input resistance is important, then a MOS differential pair will be more attractive.

b. The current source or sink

A simple current sink or source may be created by a MOS transistor in the configurations shown in Figure 13 and Figure 14, respectively. The sink is designed to operate in the MOS transistor's saturation region. From Figure 13, the voltage across the transistor must be above V_{min} in order for transistor to be in saturation. The current source also uses the MOS transistor's saturation region. The current source will only be valid for values of v_O given by

$$v_o \leq V_G + |V_T| - V_{ss} \qquad \text{(Eq 4.14)}$$
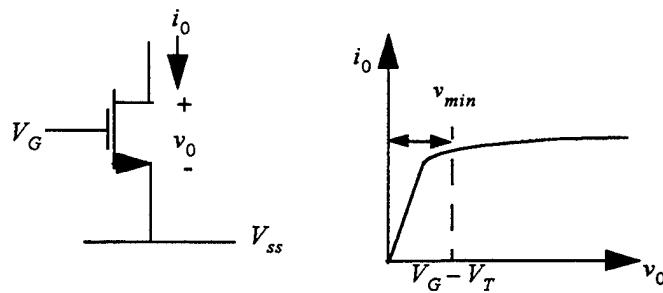
Figure 13: Current sink and its characteristics [Ref. 8 p. 219]

These configurations have the advantage of being very simple. One disadvantage is that the small signal output resistance may not be enough for some applications that require a more constant current. In addition, these configurations provide too narrow of a voltage range for some applications. However, for most applications, their performance will be adequate.

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c. The current mirror

The current mirror comes immediately following the differential amplifier as being the most useful of all analog circuits. It is used to multiply a reference current produced by a current source. It uses the principle that if the gate to source voltages are the same for two identical MOS transistors, then their channel currents should be the same. A basic current mirror circuit is shown in Figure 15.
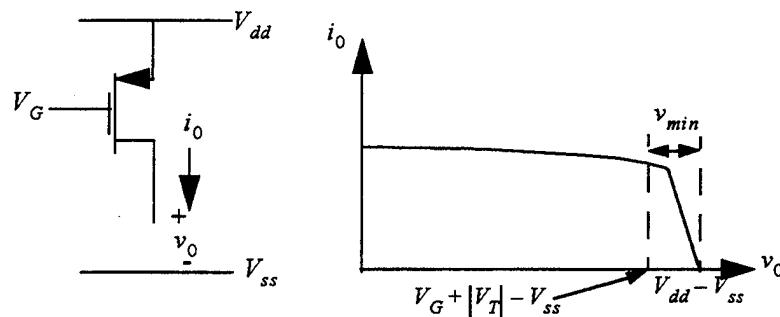

Figure 14: Current Source and its characteristics [Ref. 8 p. 220]
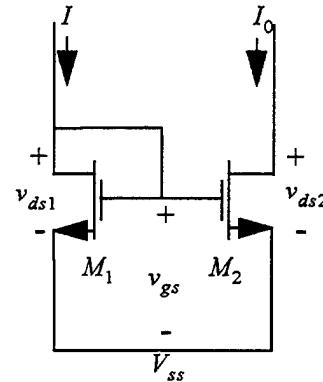

Figure 15: The basic current mirror circuit [Ref. 8 p. 227]

M_1 is in saturation because $v_{ds1} = v_{gs}$. M_2 is also in the saturation region if it is assumed that

$$v_{ds2} \geq v_{gs} - V_{T2} \qquad \text{(Eq 4.15)}$$

The ratio of I_0 to I becomes

$$\frac{I_o}{I} = \frac{\beta_2 (V_{gs} - V_{T2})^2}{\beta_2 (V_{gs} - V_{T1})^2} \qquad \text{(Eq 4.16)}$$

If one substitutes the definition of β and eliminates common process dependent terms, the above equation becomes

$$\frac{I_o}{I} = \frac{\left(\frac{W_2}{L_2}\right)}{\left(\frac{W_1}{L_1}\right)} = \frac{W_2 L_1}{W_1 L_2} \qquad \text{(Eq 4.17)}$$

Thus, the output current I_O is a multiple of the reference current I, and the multiplicative factor is determined by the relative geometry of the transistors, M_1 and M_2.

2. The High Gain Stage

The differential input stage rarely provides enough gain so it must be augmented by a high gain stage. A CMOS comparator known as the current sink/source inverter is commonly used as a second gain stage. Figure 16 shows a simple inverting comparator and its dc transfer curve. The trip voltage is described by the following equations

$$V_{TRP} = V_{ss} + \left[\frac{2I_B}{\beta_2 \left[1 + \lambda_2 \left(\frac{V_{dd} - V_{ss}}{2} \right) \right]} \right]^{1/2} + |V_{T2}| \qquad \text{(Eq 4.18)}$$

$$I_B = \frac{\beta_2}{2} (V_{BIAS} - V_{dd} - V_{T1})^2 \left[1 + \lambda_1 \frac{(V_{dd} - V_{ss})}{2} \right] \qquad \text{(Eq 4.19)}$$
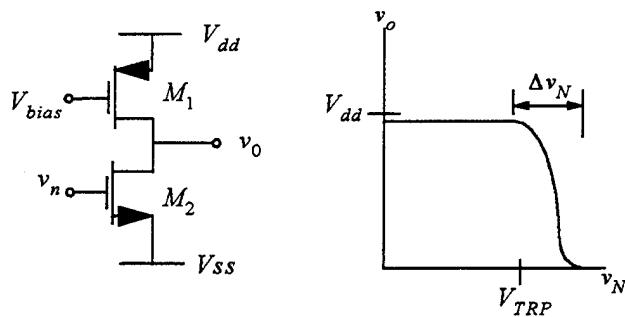
Figure 16: A simple inverting comparator and its dc transfer curve [Ref. 8 p. 327]

The term λ is the channel length modulation parameter. The problem with this comparator is that its trip voltage cannot be predicted as it is dependent upon the supply voltages. The trip voltage of the differential input stage is, however, very predictable. To make the two complement, the limited output range of the differential stage must be centered at the trip voltage of the inverting comparator.

Finally, the gain of the inverter can be described according to the relation below

$$A_V = -\left[2\frac{\beta_2}{I_B}\right]^{1/2} \frac{1}{\lambda_1 + \lambda_2}.$$
(Eq 4.20)

3. The Output Buffer Stage

The role of the output stage is to provide the amplifier with a low output resistance so it can deliver the output signal to the load without loss of gain. One should remember that an ideal op amp has a zero output impedance. The output stage is the final stage of the op amp and so it deals with relatively large signals. The most common output stage is the emitter (BJT) or the source (MOS) follower.

The source follower circuit is shown in Figure 17. The configuration has both a large current gain and a low output resistance. Through the use of small signal analysis, the output resistance of a source follower is found to be

$$R_o \cong \frac{1}{g_m}$$
(Eq 4.21)

which is normally low.

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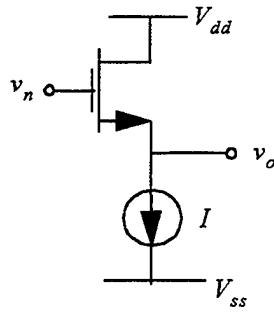
Figure 17: Source follower output amplifier

The open circuit voltage gain is given by

$$A_{vo} = \frac{1}{1 + 1/(g_m r_o)}$$

(Eq 4.22)

The term r_o is the output resistance of the transistor, given by

$$r_o = \frac{V_A}{I_d}$$

(Eq 4.23)

where V_A is the Early voltage. Since $g_m r_o$ is usually large, the gain is nearly unity.

The range of the output signal swing is a disadvantage here. The maximum value of v_o is

$$v_{omax} = V_{dd} - V_T$$

(Eq 4.24)

because of the common-source M_2 and the constant gate voltage. The problem is that V_{T1} is dependent on the output voltage because of the body effect [Ref. 9]. V_{T1} can be approximated by the relation

$$V_T \cong V_{TO} + \gamma \, (v_{SB})^{\frac{1}{2}}$$

(Eq 4.25)

The substitution of Eq. 4.25 into Eq. 4.24 and solving for v_o results in

$$v_{omax} \cong V_{dd} + \frac{\gamma}{2} - V_{TO} - \frac{\gamma}{2} \left[\gamma^2 + 4 \, (V_{dd} - V_{ss} - V_{TO}) \right]^{\frac{1}{2}}$$

(Eq 4.26)

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The term V_{TO} is the initial threshold voltage and γ is the body effect coefficient. With $V_{ss} = -V_{dd} = 5V$, v_{omax} approaches only 1 V.

Another common output stage is the push-pull inverting amplifier which is very efficient and can sweep nearly the entire voltage range of V_{dd} to V_{ss} but gives no reduction in output resistance.

4.   Frequency Compensation

Operational amplifiers are frequently used in a negative feedback configuration. It is important that this feedback be stable and does not cause oscillations or clamping. This stability can be determined by the phase of the response when the magnitude of the response is unity. Figure 18 called a bode plot demonstrates this graphically.
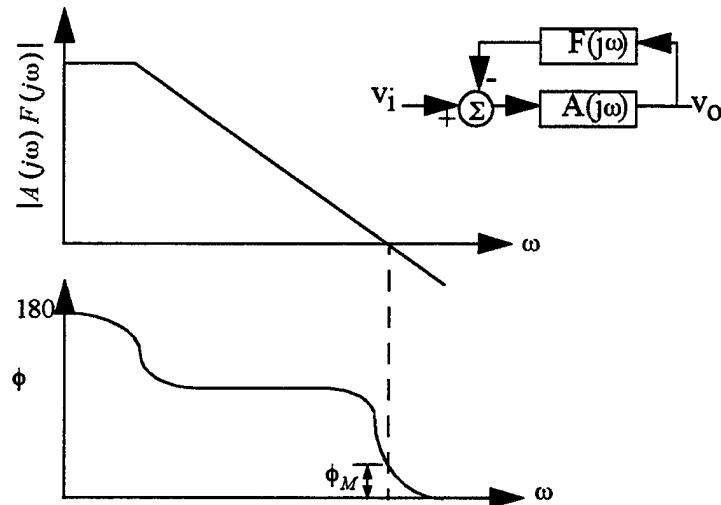

Figure 18: Frequency response of a negative feedback system [Ref. 8 p. 376]

ϕ_M is called the phase margin. Figure 19 shows how greater phase margin means less "ringing" of the output response.

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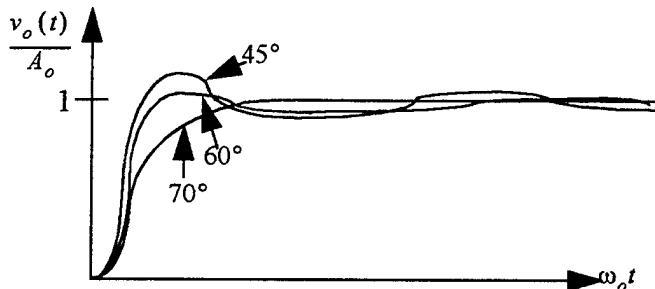
Figure 19: Response of a second order system [Ref. 8 p. 376]

For an op amp, it is desirable that the phase margin be at least $45°$. Figure 20 shows the bode plot for a typical uncompensated op amp. The frequencies labeled are called poles. The poles are frequencies at which a parasitic capacitance or resistance causes the frequency response to change slope. The angular frequency of the poles is given by

$$\omega_p = \frac{1}{R_o C_o} \qquad \text{(Eq 4.27)}$$

where R_o and C_o are the resistance and capacitance as seen from the output of an amplifier stage. Typically, these poles are of high frequency and are relatively close together. The phase margin, in most cases, is much smaller than $45°$. Thus, some frequency compensation must be performed.

The most common method of compensation is known as pole splitting or the Miller compensation technique. It is applied by connecting a feedback capacitor to an inverting stage in the amplifier. This capacitance changes the angular frequency of the first pole to

$$\omega_{p1} \cong \frac{1}{g_m R_{o2} C_C R_{o1}} \qquad \text{(Eq 4.28)}$$

and the second pole to

$$\omega_{p2} = \frac{g_m C_C}{C_{o1} C_{o2} + C_C (C_{o1} + C_{o2})}. \qquad \text{(Eq 4.29)}$$

It can be shown that as C_C is increased, ω_{p1} will be reduced and ω_{p2} will be increased. The poles become farther apart or split. This effectively makes the phase margin wider as shown in Figure 21.

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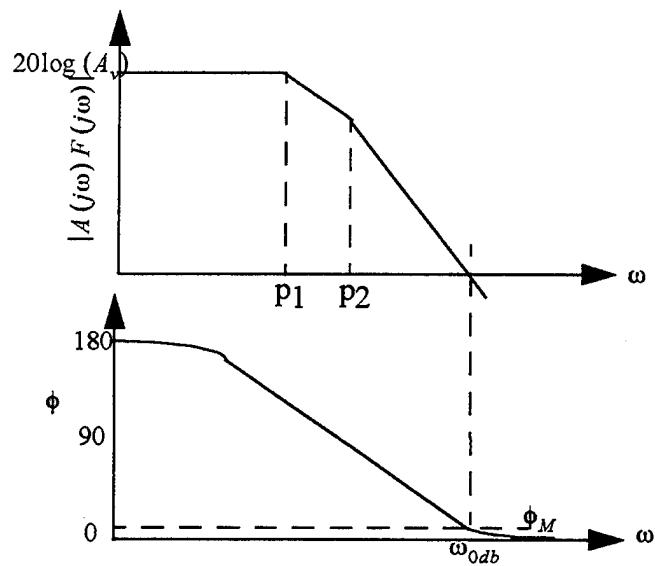
**Figure 20: Frequency response of an uncompensated op amp [Ref. 8 p. 378]**
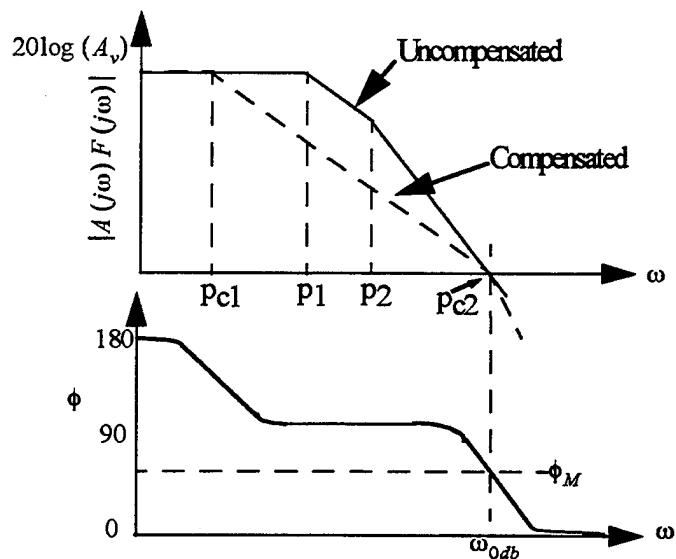
Figure 21: Compensated frequency response of an op amp [Ref. 8 p. 380]

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The value of C_C should be only large enough to get the desired phase margin, since capacitors consume large amounts of area in integrated circuit technology. [Ref. 3 pp. 632-634]

Lastly, the gain of the amplifier is moderately reduced by the frequency compensation. This is unavoidable if a more stable op amp is desired. This is another reason for keeping the compensating capacitor as small as possible.

5. Bias Circuit

The bias circuit distributes the required bias currents to the various stages of the op amp for proper operation. It does this by using a current source as a reference current and uses current mirrors to direct the required multiples of the reference to the various stages. The operation of both the current source and the current mirror was described in Chapt. IV.D.1.b and Chapt. IV.D.1.c, respectively.

V. THE LOW VOLTAGE PSEUDO-BICMOS OP AMP

A. THE DESIGN

The op amp chosen for fabrication is based on a design by Holman and Connelly of the Georgia Institute of Technology [Ref. 1]. Their design was fabricated in a 1.2 μm n-well CMOS process and has achieved good results. The modified version of their low voltage, pseudo-BiCMOS op amp is shown in Figure 22. All values of resistors and capacitors were resized in order to improve stability.
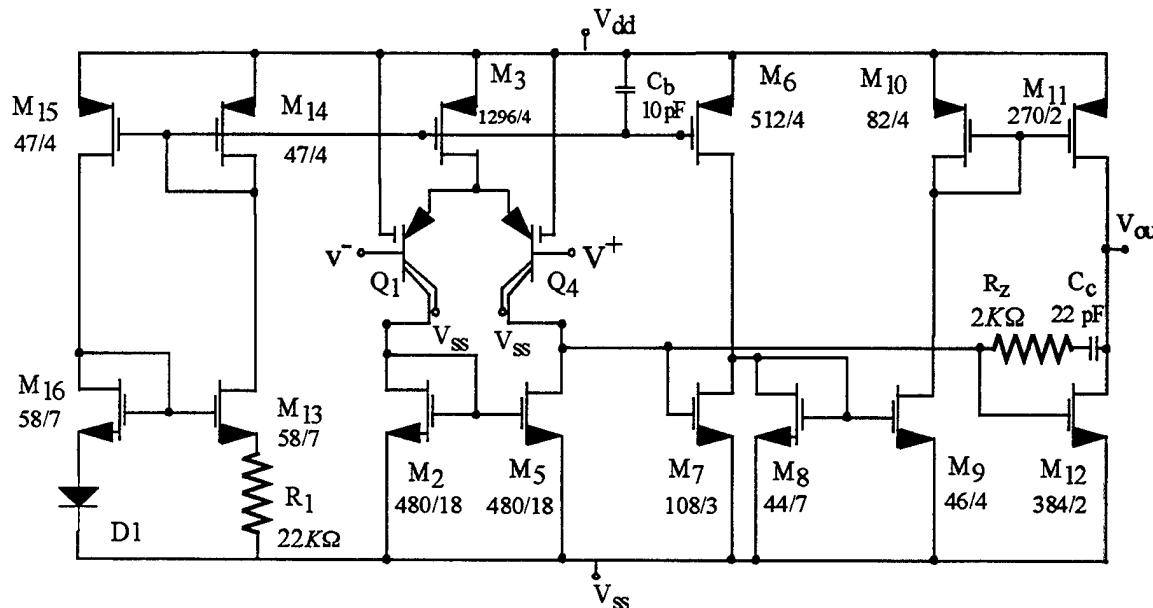
Figure 22: The pseudo-BiCMOS op amp

1. Differential Transconductance Stage

The input differential amplifier is built with parasitic lateral BJTs. To keep the current at a low enough level for the emitter dot structure, 40 emitter dot structures are connected in parallel to form one transistor. This is evident in Figure 23, which is the MAGIC layout
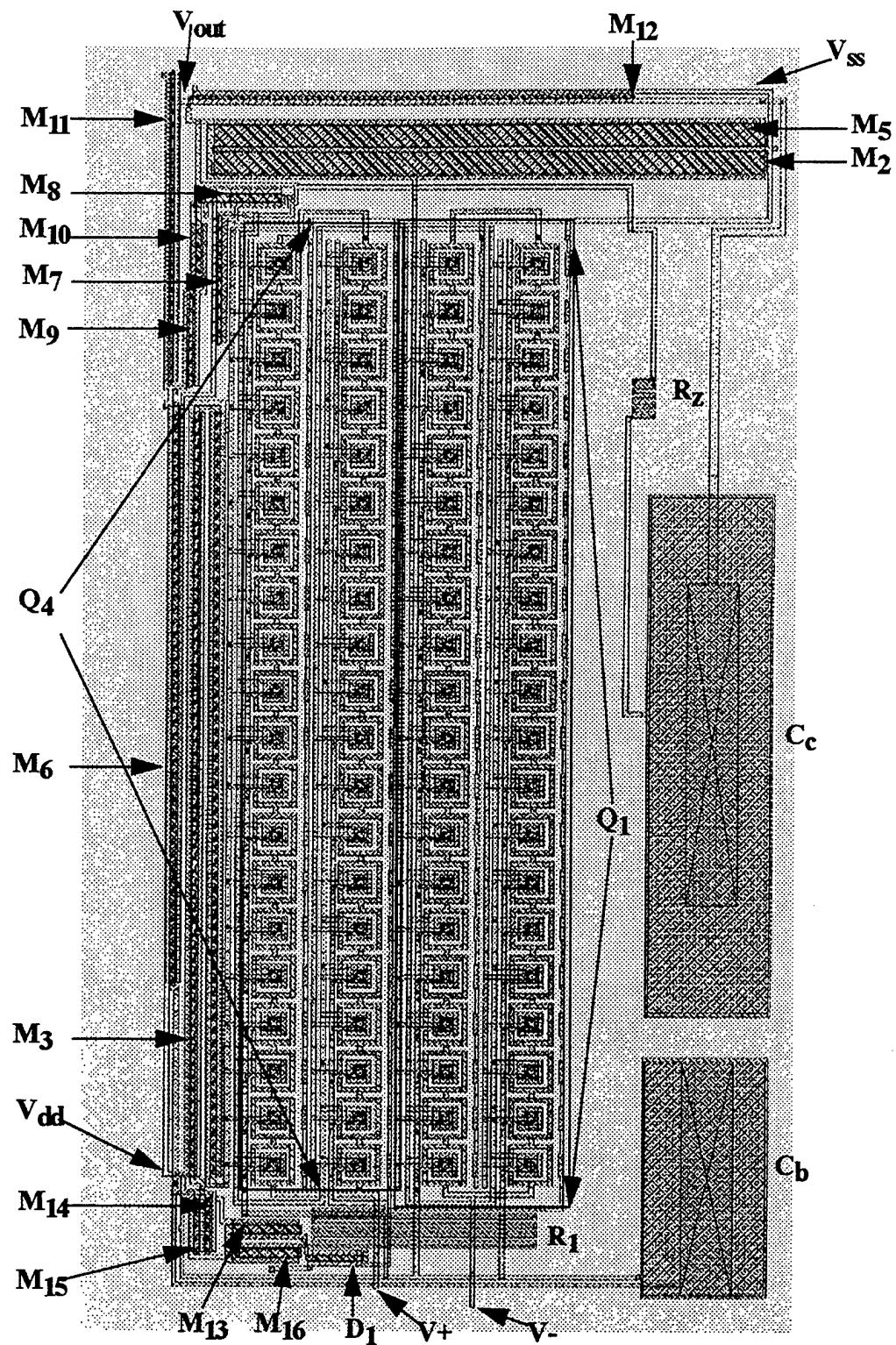
Figure 23: MAGIC layout of the BiCMOS operational amplifier

of the op amp. These transistors occupy a large area of the chip. For this reason, lateral BJTs were only used where they would have the most effect. Since the design seeks high gain and low input noise, the lateral BJTs are placed in the input stage.

The lateral BJT differential amplifier is biased by a current mirror which is fed by a current source (M_3). The transistors here have extremely large width-to-length ratios to reduce the input noise as well.

2.   High Gain Stage

The high gain stage is a CMOS inverter which adds to the gain of the differential stage. The width-to-length ratios of these transistors are also large. The p-MOS transistor width is four times the n-MOS transistor width since p-MOS carrier mobility is less than n-MOS carrier mobility. This balances the current gain β of the transistors. An inverter has the sharpest voltage transition when β of its transistors are equal.

3.   Output Buffer Stage

The output buffer stage is a push-pull source follower. This type of buffer has low output resistance and is capable of high slew rate performance at high frequencies. Once again, the width-to-length ratios of the transistors are large.

4.   Frequency Compensation

The resistors and capacitors which provide the frequency compensation have been resized from the Holman and Connelly design. PSPICE simulations of their design showed it to be unstable. Values for the resistor and capacitor sizes were determined by trial and error to achieve a phase margin of 45 degrees and yet have a unity gain frequency of greater than 2 MHz. This is the cause of the reduced gain bandwidth product and slew rate.

5.   Bias Circuit

The bias circuit is a diode-based bootstrapped circuit. Although bias circuits of this type often require a start-up circuit to ensure proper operation, no problems have been encountered in simulation due to the lack of a start-up circuit. [Ref. 10]

B. THE MAGIC LAYOUT

The amplifier was laid out for manufacturing in the MOSIS process using MAGIC VLSI layout software. The layout was based on a structural hierarchy as depicted in Figure 24.

```
                    ┌─────────────────────────┐
                    │  Four Amplifier Pad Ring │
                    └─────────────────────────┘
                              ▲
                    ┌─────────────────────────┐
           ┌───────▶│ BiCMOS Operational Amplifier │◀───────┐
           │        └─────────────────────────┘             │
  ┌──────────────────┐  ┌─────────────────┐  ┌──────────────────┐  ┌────────────────────┐
  │Polysilicon Resistors│ │CMOS Transistors│  │Lateral BJT Transistors│ │Dual Poly Capacitors│
  └──────────────────┘  └─────────────────┘  └──────────────────┘  └────────────────────┘
                                                      ▲
                                             ┌─────────────────────┐
                                             │ Emitter Dot Structures │
                                             └─────────────────────┘
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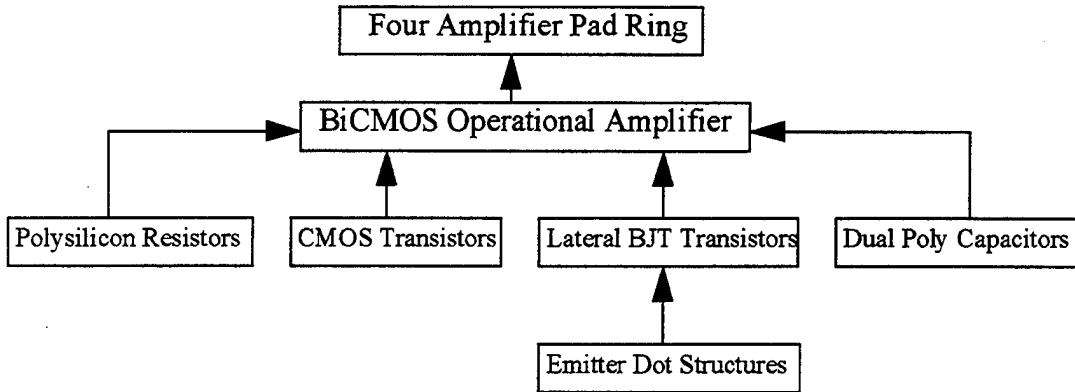
Figure 24: Structural hierarchy of MAGIC layout

The emitter dot structure is built in an n-well to construct a pnp bipolar device. The pnp transistor in Figure 22 is realized by 40 of these structures connected in parallel. The emitter dot structure is shown in Figure 25.

The diode is realized by connecting the drain of a n-MOS transistor to its gate. A transistor with the same width-to-length ratio as M_9 was used to create the diode.

The capacitors are built from a sandwich of two different polysilicons separated by an insulating oxide layer. The area required for the capacitor is computed from the capacitance between the two layers of silicon, which is 474 atto-farads per square micron.

Resistors were built from gate polysilicon which has a resistance of 21.7 Ω/(square area). Typically, the resistance realized from the CMOS process has an inaccuracy of $\pm$ 20%. Snaking the polysilicon aided in realizing the long length, reducing the area required for the resistance values in the design.

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The pad ring used is a standard analog type. It was used because the development of a tailored pad ring would be time consuming. The four amplifier pad ring layout is displayed in Figure 26.
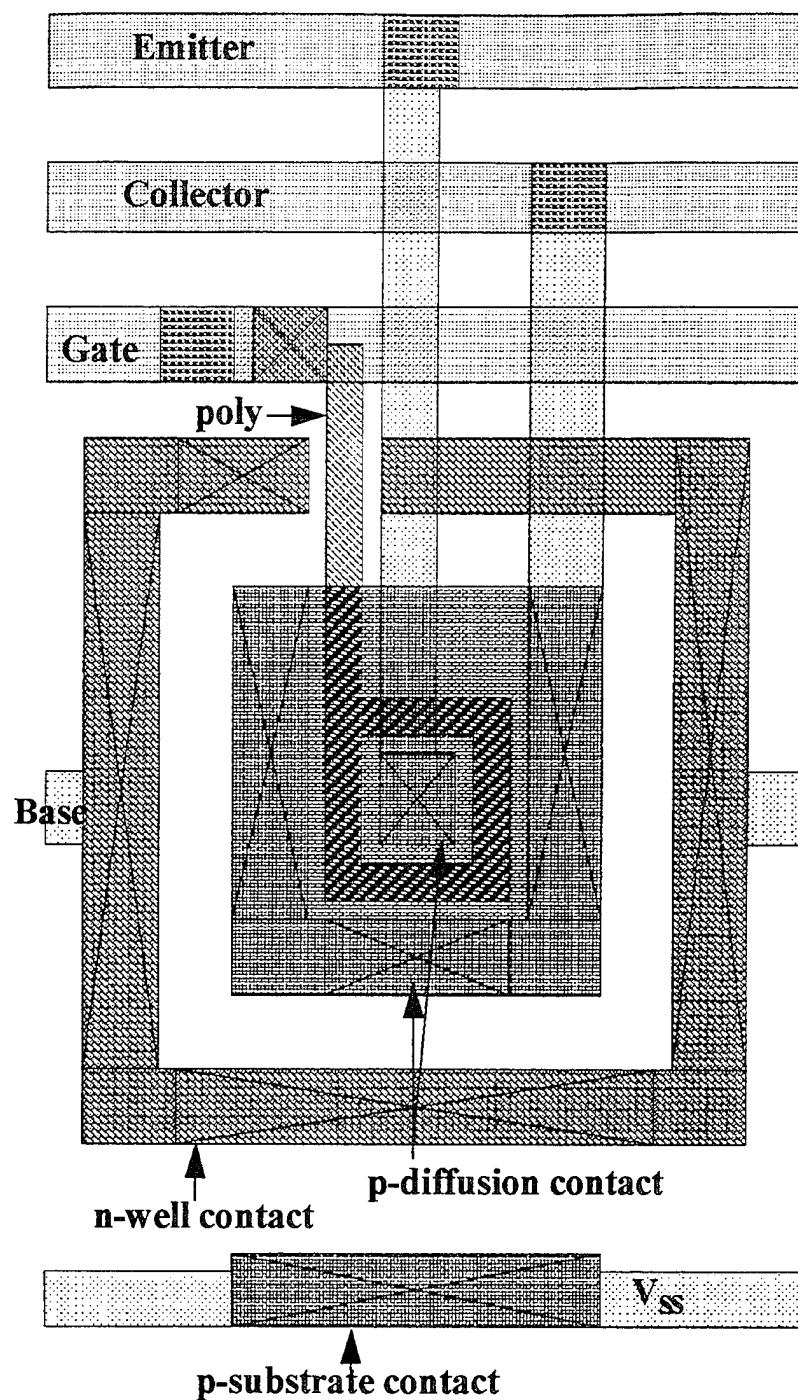
Figure 25: The emitter dot structure
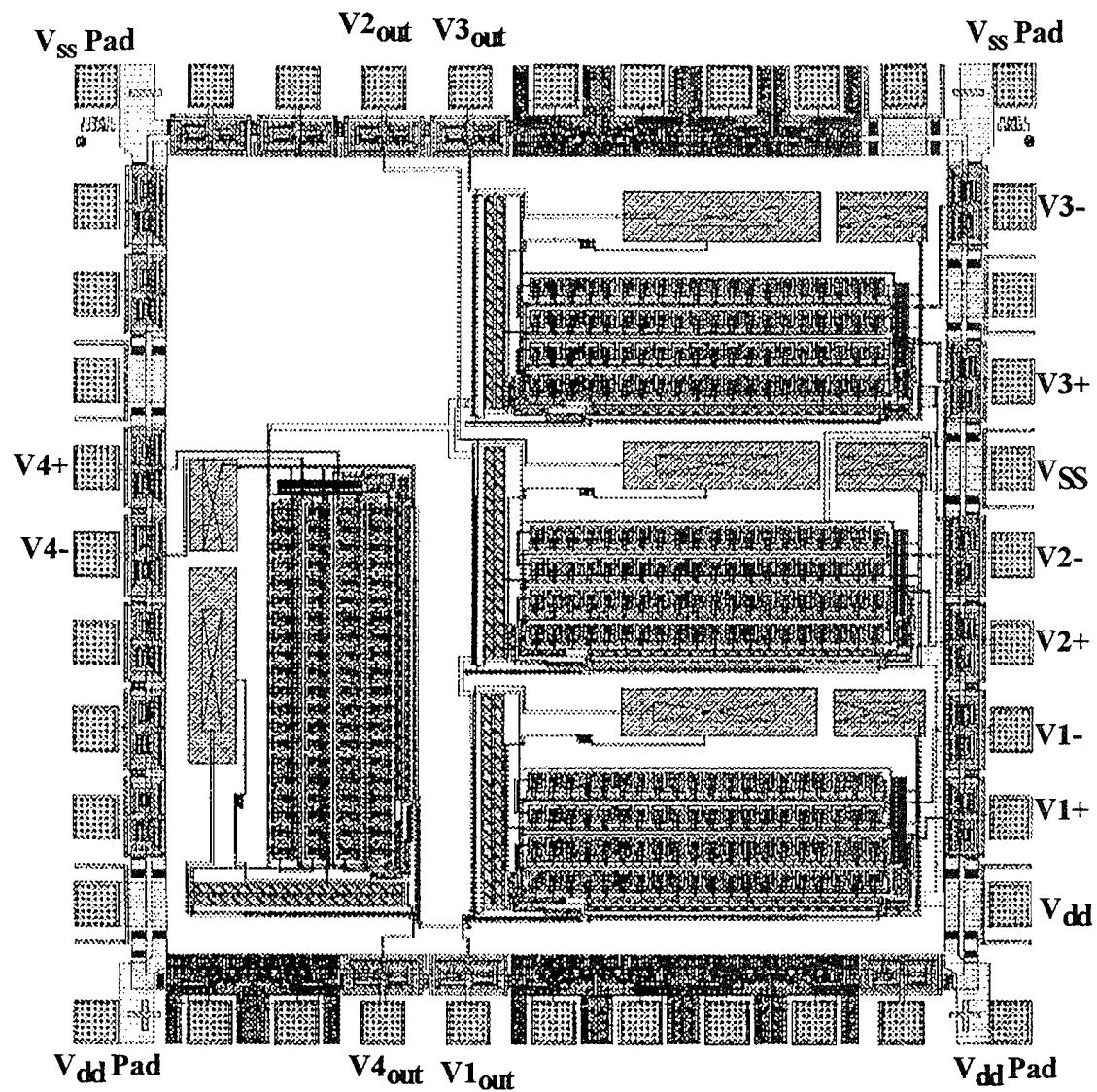
Figure 26: The four amplifier pad ring

VI. SIMULATION AND ANALYSIS

The performance of the pseudo BiCMOS op amp was simulated and analyzed with PSPICE analog simulation software by Microsim Corp. SPICE models for the MOS transistors were obtained from MOSIS process specifications. The SPICE model for the lateral parasitic bipolar was obtained from W. Timothy Holman of Georgia Institute of Technology.

Simulation was conducted to determine all common open loop and closed loop characteristics of the op amp. The PSPICE simulation code is contained in Appendix A.

A. OPEN-LOOP SIMULATION

The open loop configuration has the inverting node grounded and uses the op amp in a unity gain configuration as the load as shown in Figure 27. Inputs were placed at the non-inverting node to get the required ac or dc characteristics. Power supply voltage used was ± 2.5 V.
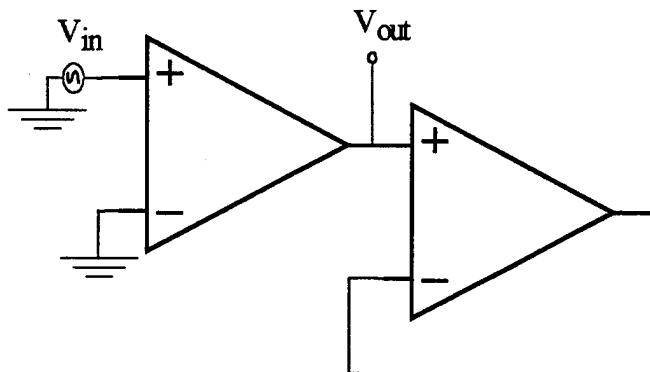
Figure 27: The open-loop simulation configuration

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1. Open Loop dc Transfer Characteristics

The open loop transfer curve for the op amp is shown in Figure 28. Notice that the output signal is not zero volts for a zero volt input. This is the effect of the input offset voltage. An effective method to find the input offset voltage is to connect the op amp in the unity gain configuration and connect a constant dc voltage to the non-inverting input. The difference between the input and output voltage is the offset voltage. This was found to be 511 μ V. Correspondingly, input offset current is 3.029 μ A. Figure 29 shows the dc transfer curve after the offset voltage is applied.
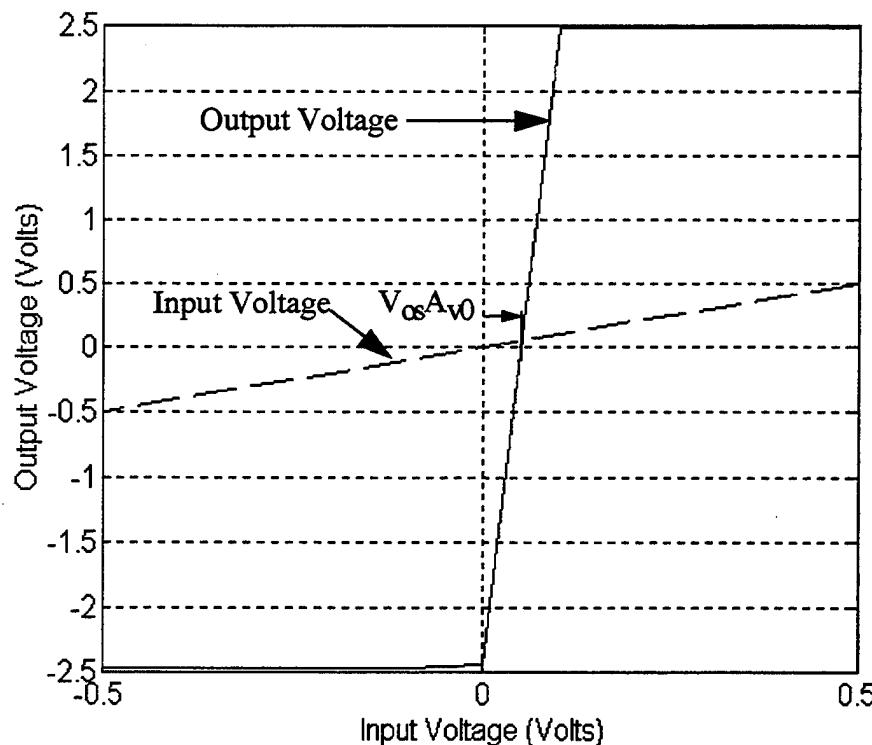
**Figure 28: Open-loop transfer characteristic**

The open loop simulation by PSPICE estimates the input resistance of the op amp at 10 KΩ. This resistance is very low because lateral BJTs are being used at the input. If MOS transistors were used at the input, the input resistance would be almost infinite. Despite this

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drawback, the BJT is used because of its better gain and also since it improves the input noise. The output resistance was estimated to be 147 Ω. This is a small resistance that compares favorably with other op amps. Power dissipation is found to be at 13.4 mW.
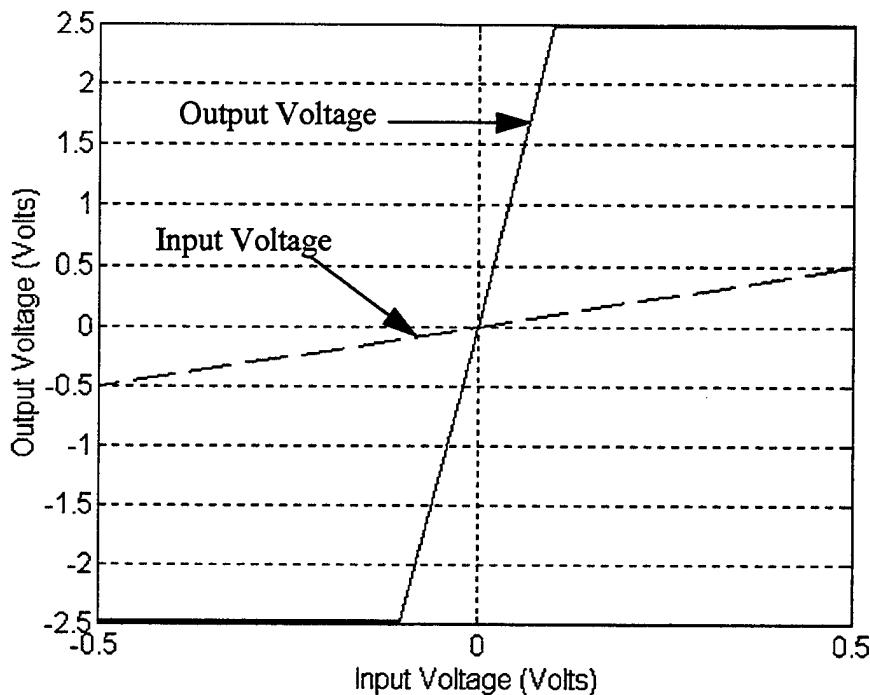

Figure 29: Open-loop transfer characteristic with offset voltage applied

2. Open-loop Frequency Response

The open loop magnitude response is shown in Figure 30. The input was 10 mV, which corresponds to -40 dB. Open loop gain was found to be 33.8 dB, which is the difference between the input and the simulated output in decibels, as shown in Figure 30. The unity gain frequency, also known as the gain bandwidth product, is 4.35 MHz. The corresponding phase margin is 45 degrees. The original design by Holman and Connelly was found to be unstable. Additional phase margin was created by resizing all resistors and capacitors. This, of course, reduced the gain bandwidth product substantially from what

was originally expected. Still, the op amp performs reasonably well with a ± 2.5 V power supply.

Compared to a purely CMOS design of equivalent topology, this op amp has only a fraction of the open-loop gain [Ref. 10]. However, since op amps are used primarily in closed loop circuits, this configuration will be empahsized.

3.   Power Supply Range and PSRR

The lowest power supply voltage at which the amplifier will operate is ± 0.6 V. The unity gain bandwidth is 570 kHz at this power supply voltage level. Open loop gain is 43.69 dB. Figure 31 shows how unity bandwidth varies with power supply voltage. Power supply voltage's effect on open-loop gain is shown in Figure 32. One can note that at power supply voltages of 0.65 to 0.83, there is an abnormality. Between these voltages there is usually high open-loop gain. However, it is too a narrow window to be very useful.

There is also another window between 3.5 V and 10 V where open-loop gain is maximized. A maximum gain of 88.7 dB is achieved by powering the amplifier with ±6 V. Increasing power supply voltage will increase bandwidth at a predictable rate.

From the above results, it is not surprising that the power supply rejection ratio (PSRR) is very poor. At a supply voltage of ± 2.5 V, the positive PSRR is only 12.39 dB. The negative PSRR is even lower at 2.35 dB. Thus, the output voltage will be very susceptible to noise in the power supply.

Op amps of an equivalent CMOS design normally enjoy a PSRR of -132 dB, which is obviously many times less than the proposed design [Ref. 10].
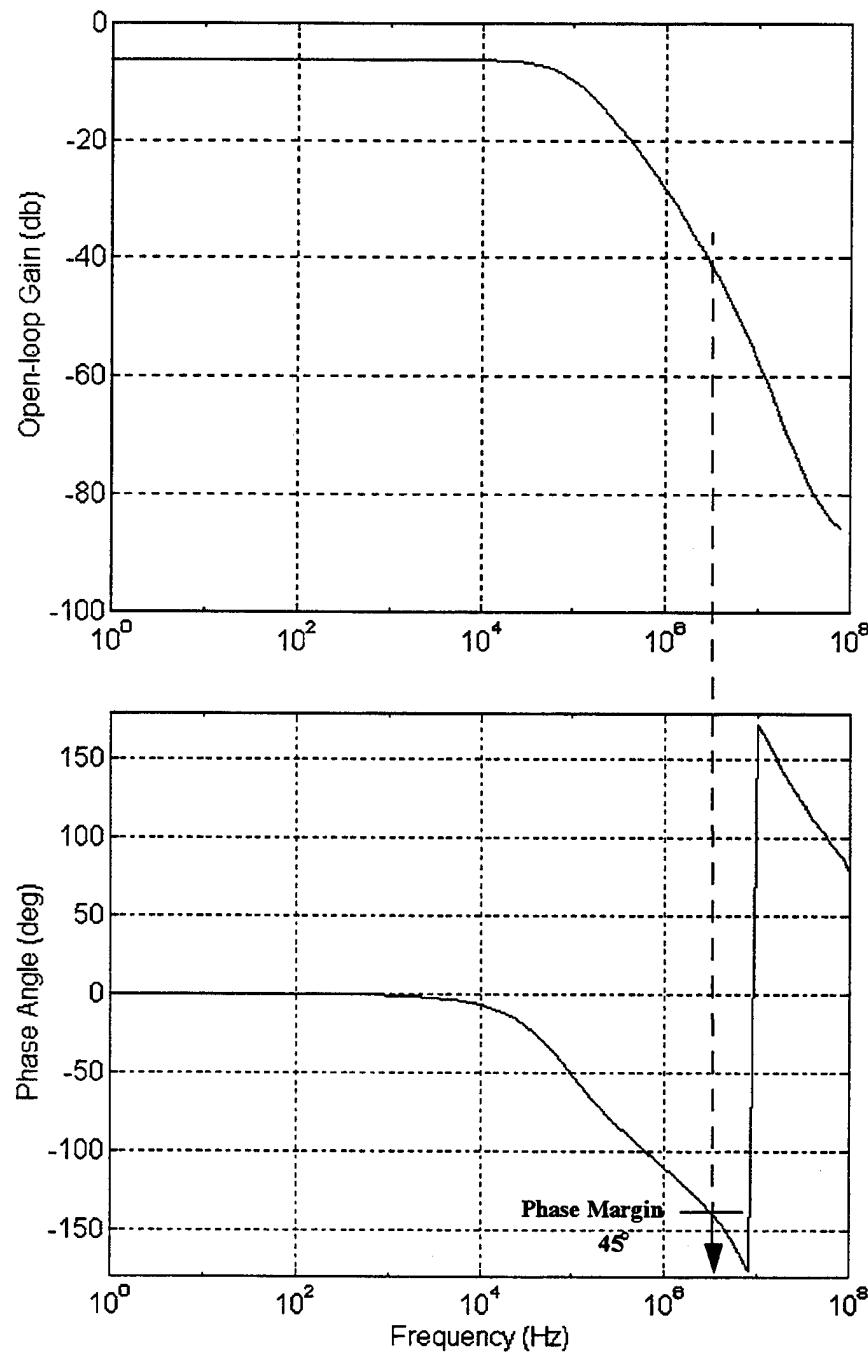
Figure 30: Open loop magnitude response
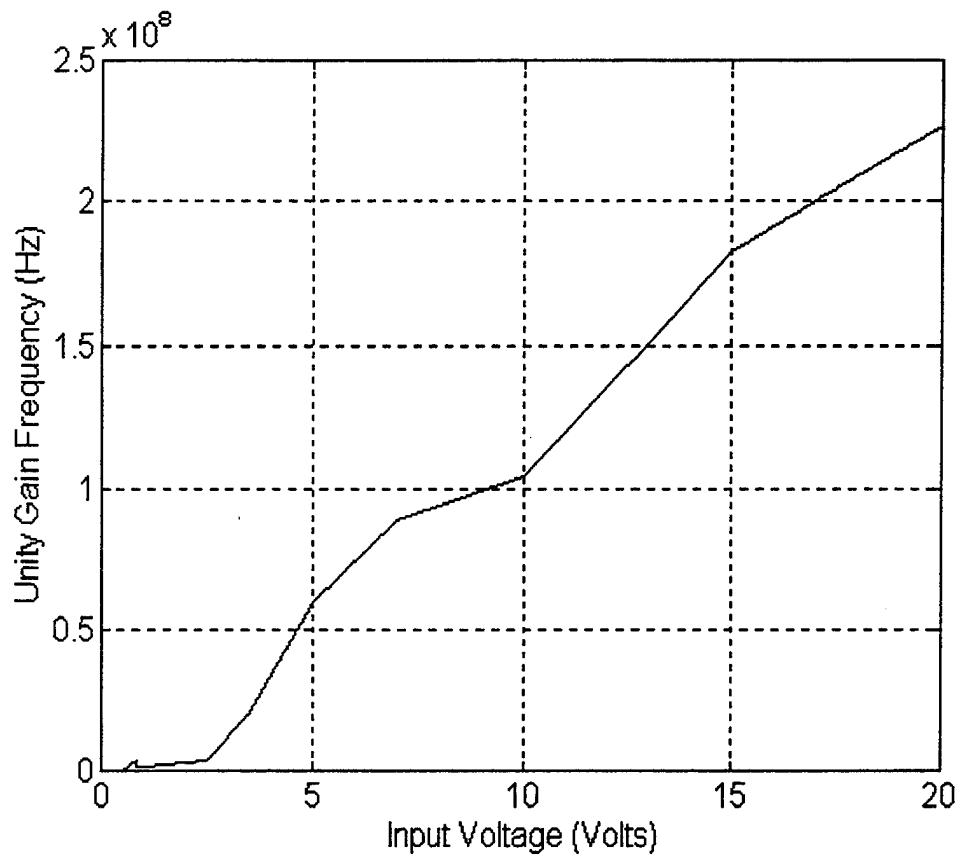
Figure 31: Unity gain frequency as affected by power supply voltage
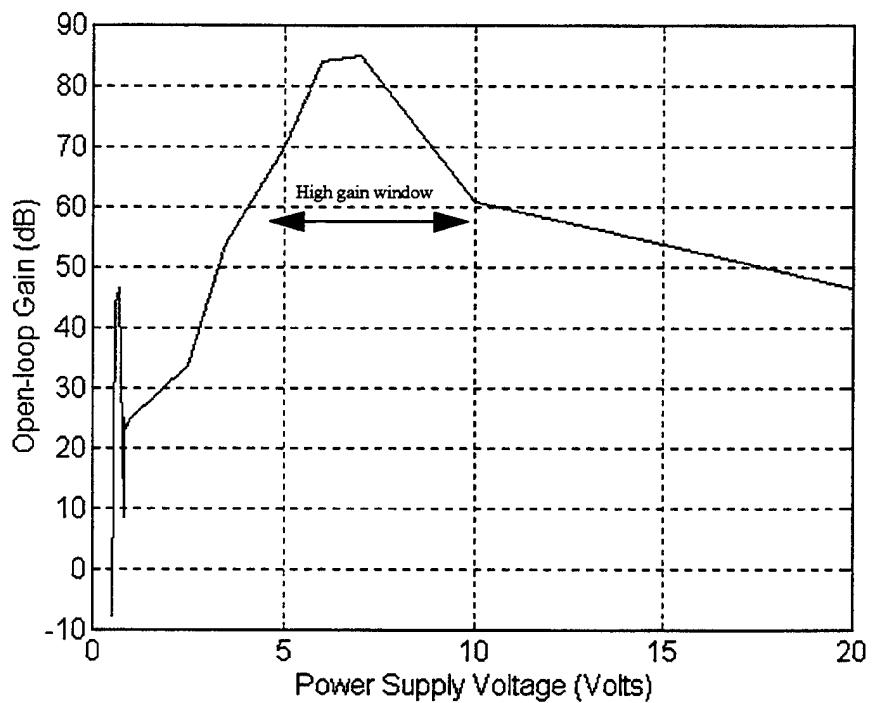
Figure 32: Power supply voltage's effects on open-loop gain

4. Common Mode Gain and CMRR

The common mode gain is a frequency dependent parameter. Table 2 below shows the common mode gain and the CMRR of the amplifier powered by ± 2.5 V.

Frequency	Common Mode Gain (dB)	CMRR (dB)
1 K	1.8	28.6
10 K	-9.95	43.7
100 K	-28.9	59.2
1 M	-41.4	52.7

Table 2: Common mode gain and CMRR

The CMRR is very low at low frequencies. This is directly opposite of what was expected. The reason for this is unknown. It is acceptable above 1 kHz but a modification for improvement would be recommended.

B. CLOSED-LOOP SIMULATION

The op amp is used most often in the negative feedback configuration. Therefore, it is important to investigate its performance in the closed loop configuration.

1. Unity Gain

Figure 33 shows the unity gain configuration. This is the most basic of the closed loop
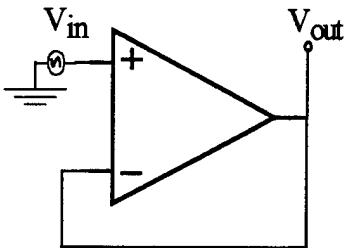

Figure 33: The unity gain configuration

applications. It is also the most demanding because its feedback is 100%. Phase margin in this configuration is the clearest sign of stability. Figure 34 shows the gain and the phase plot of the unity gain configuration. The highest frequency at which the op amp will operate at unity gain is 40 MHz. At this frequency, the phase deviation of the output is -154 degrees relative to the input. The phase margin is below the desired 45 degree phase margin, but the op amp is definitely stable.
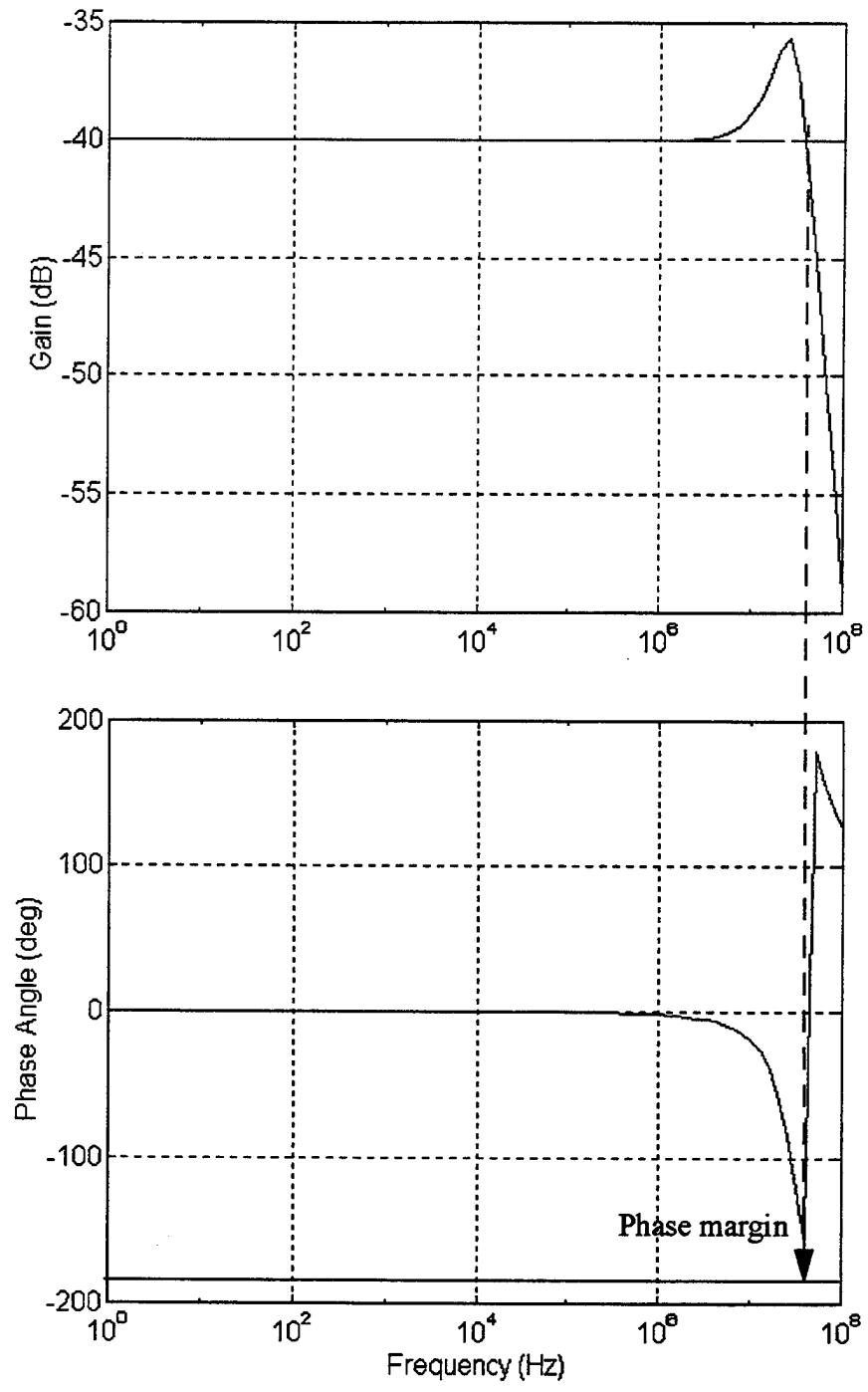
Figure 34: Unity gain frequency response

2. Slew Rate

The slew rate is also tested in the unity gain configuration. A square pulse of 1.5 V was applied to the non-inverting input to test the op amp's ability to respond to large signals. Figure 35 shows this response. The positive slew rate was found to be 11.24 V/ μs, while the negative rate was 12.02 V/μs. This is a high slew rate but much less than the slew rate of Holman and Connelly's BiLNA design. This is to be expected because this op amp has greater frequency compensation. It is, however, much better than their equivalent CMOS design. The transient response verifies the phase margin of 45 degrees.
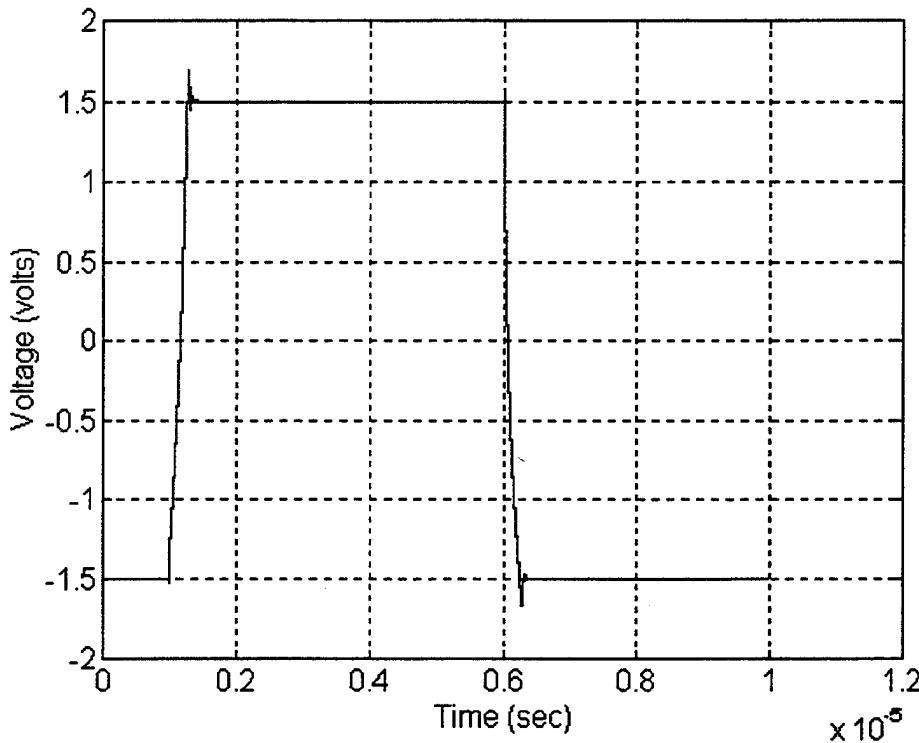

Figure 35: Slew rate of the pseudo-BiCMOS op amp

To illustrate the need for this greater frequency compensation, Figure 36 shows the slew rate simulation of Holman and Connelly's design. This design has a phase margin of -90 degrees. This is an unacceptable margin as Figure 36 shows.
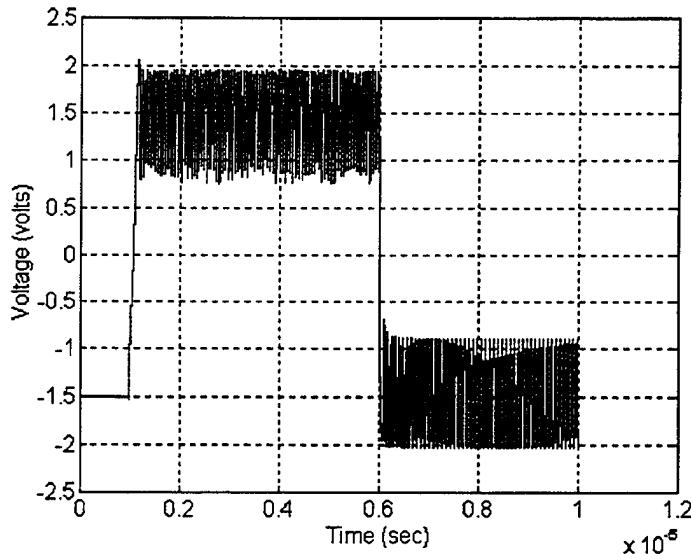
Figure 36: Slew rate of Holman and Connelly's op amp

3. Non-inverting Gain Configuration

This configuration uses negative feedback to control gain, and the output is in phase with the input. Figure 37 shows the circuit used in this application. The resistor values were chosen to achieve a gain of 10. The frequency response of this configuration is shown in Figure 38. The input signal was again set at 10 mV or -40 dB. The gain, as expected, was found to be 10.97 or 20.81 dB.
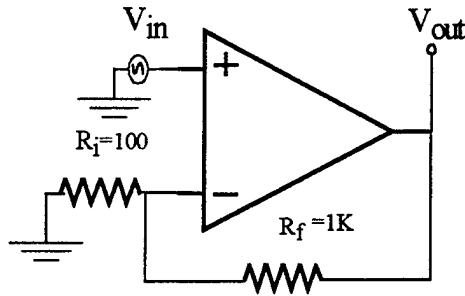
Figure 37: Non-inverting gain configuration

The -3dB frequency is 2.238 MHz. This produces a gain bandwidth product of 24.56 MHz, which is much greater than expected from the open loop computation but half of what the unity gain response suggests. The transient response shows that greater than unity gain is attained with an input of 10 mV at a frequency of 20 MHz. This is depicted in Figure 39.

4. Inverting Configuration

The inverting configuration is similar to the non-inverting one, except that the input signal is fed into the input resistor in order to achieve an inverted output. The resistor values are the same, realizing a gain of -10. Figure 40 shows the transient response of this configuration at 2.3 MHz. This demonstrates that this frequency is the - 3 db frequency. This agrees with the - 3 dB of the non-inverting configuration and therefore the gain bandwidth product is 23 MHz.
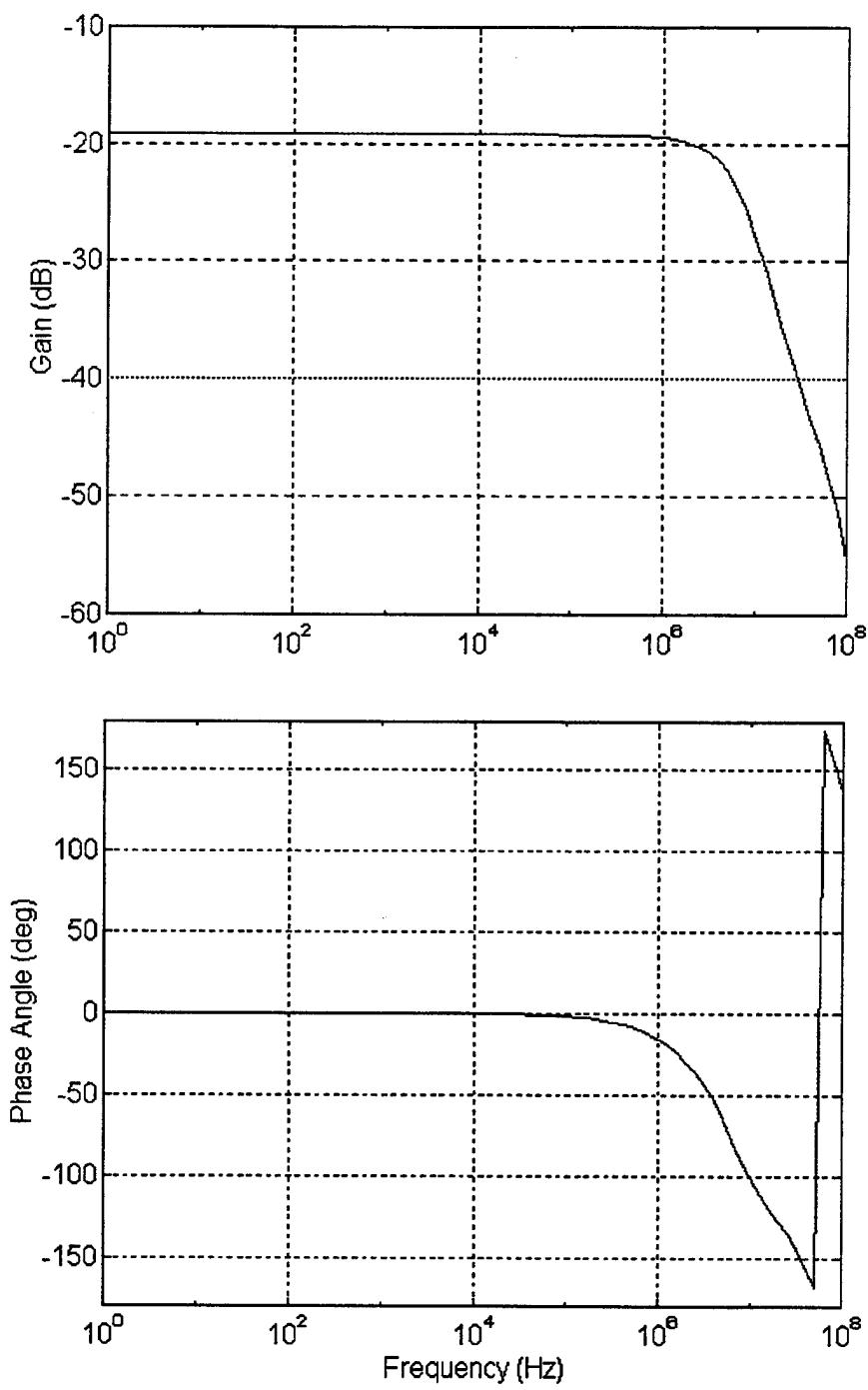
Figure 38: Frequency response of non-inverting configuration ($R_f/R_i=10$)
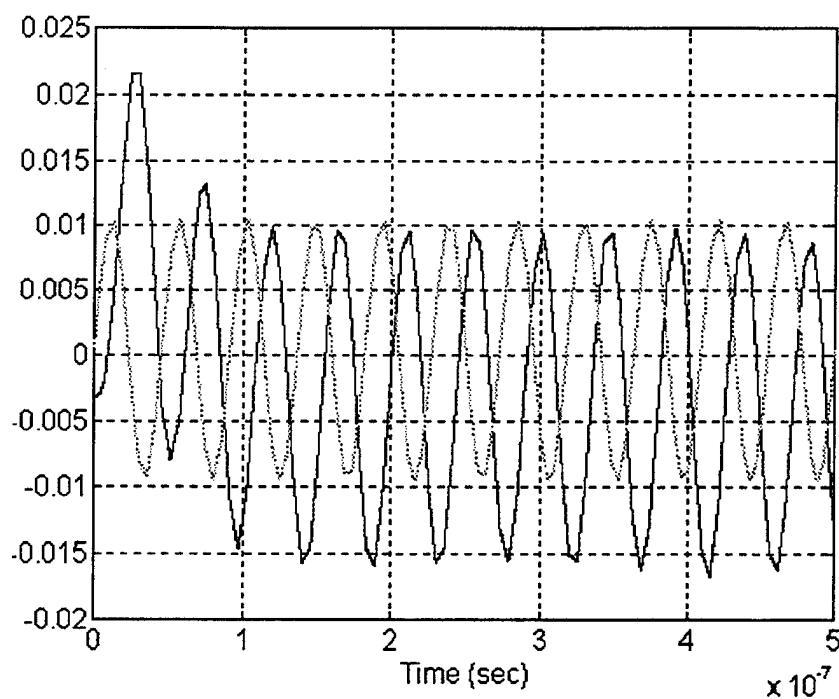
Figure 39: Non-inverting transient response   (Frequency = 20 Mhz)
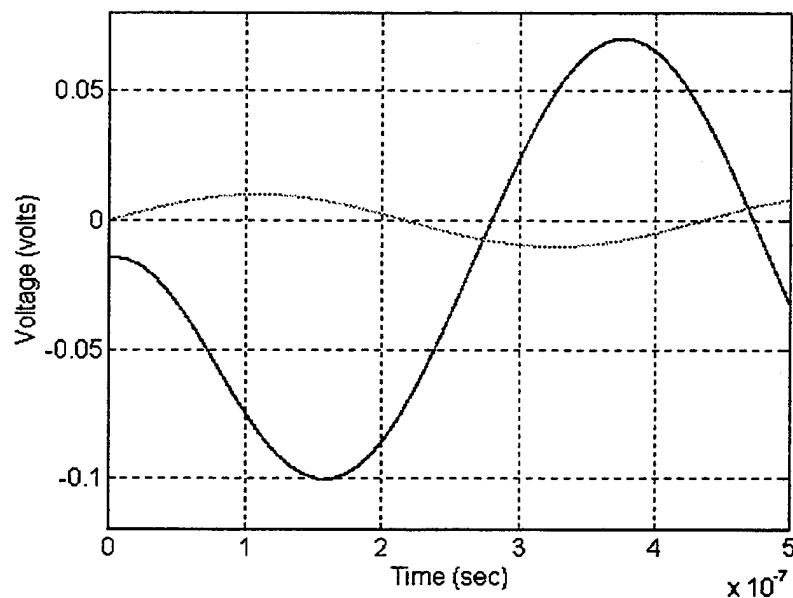
Figure 40: Inverting transient response (Frequency = 2.3 Mhz)

5. The Composite Op Amp

The composite op amp is a configuration developed by Mikhael and Michael which uses two op amps in a feedback network to realize a high performance virtual op amp [Ref. 11]. The composite op amp configuration denoted C2OA-1 is displayed in Figure 41. This configuration was simulated using the pseudo-BiCMOS op amp as the component op amps. The values for the resistors R and αR are 100Ω and 500Ω, respectively. The resulting frequency response is shown in Figure 42. The open-loop gain of this composite op amp is 1064 or 60.54 dB. This is a factor of ten folds over that of a single op amp alone. However, power dissipation was found to be 95.7 mW which is ten times the power consumption of a single op amp. Nevertheless, the composite op amp demonstrates how high performance can be achieved at low voltages.
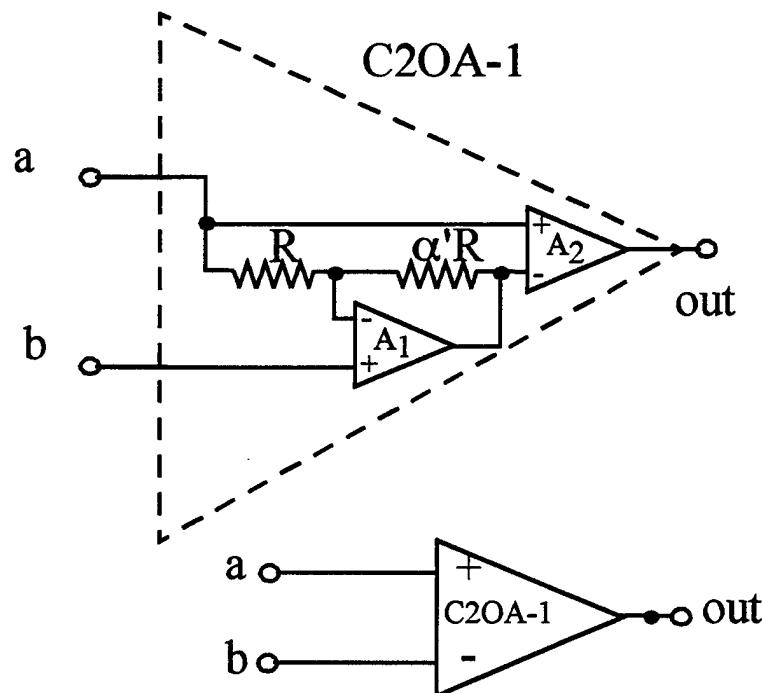
Figure 41: The Composite Op Amp

C. NOISE

The parasitic bipolar transistors were placed in the input differential stage in order to reduce input referred noise. PSPICE is capable of performing both a input and output referred noise analysis. The result of this analysis is displayed in Figure 43. The input noise voltage density at 1 Hz was found to be 2.86 nV/(Hz)$^{1/2}$, which is about eight times lower than that of Holman and Connelly's design [Ref. 1]. No reason can be given for this improvement. Perhaps, the decreased size of the resistor in the current mirror which supplies the bias current to the input differential stage is the cause. Also, the quiescent current is lower, 1.108 mA. The output referred noise density is 140 nV/(Hz)$^{1/2}$ at 1 Hz. The point at which input noise is equal to output noise was found to be 3 MHz. Noise density at this frequency is 3.18 nV/(Hz)$^{1/2}$.

The noise performance of this op amp should be better than the equivalent CMOS design. Simulation confirms these results, with the CMOS op amp having a higher noise density of 6.5 nV/(Hz)$^{1/2}$. [Ref. 10]

D. SUMMARY

A summary of the simulation results are listed in Table 3. These results are compared with the results of Holman and Connelly's BiLNA op amp and their CMOS LFA op amp [Refs. 1 and 10]. The phase margin of their BiLNA op amp shown in the table is from the PSPICE simulation.
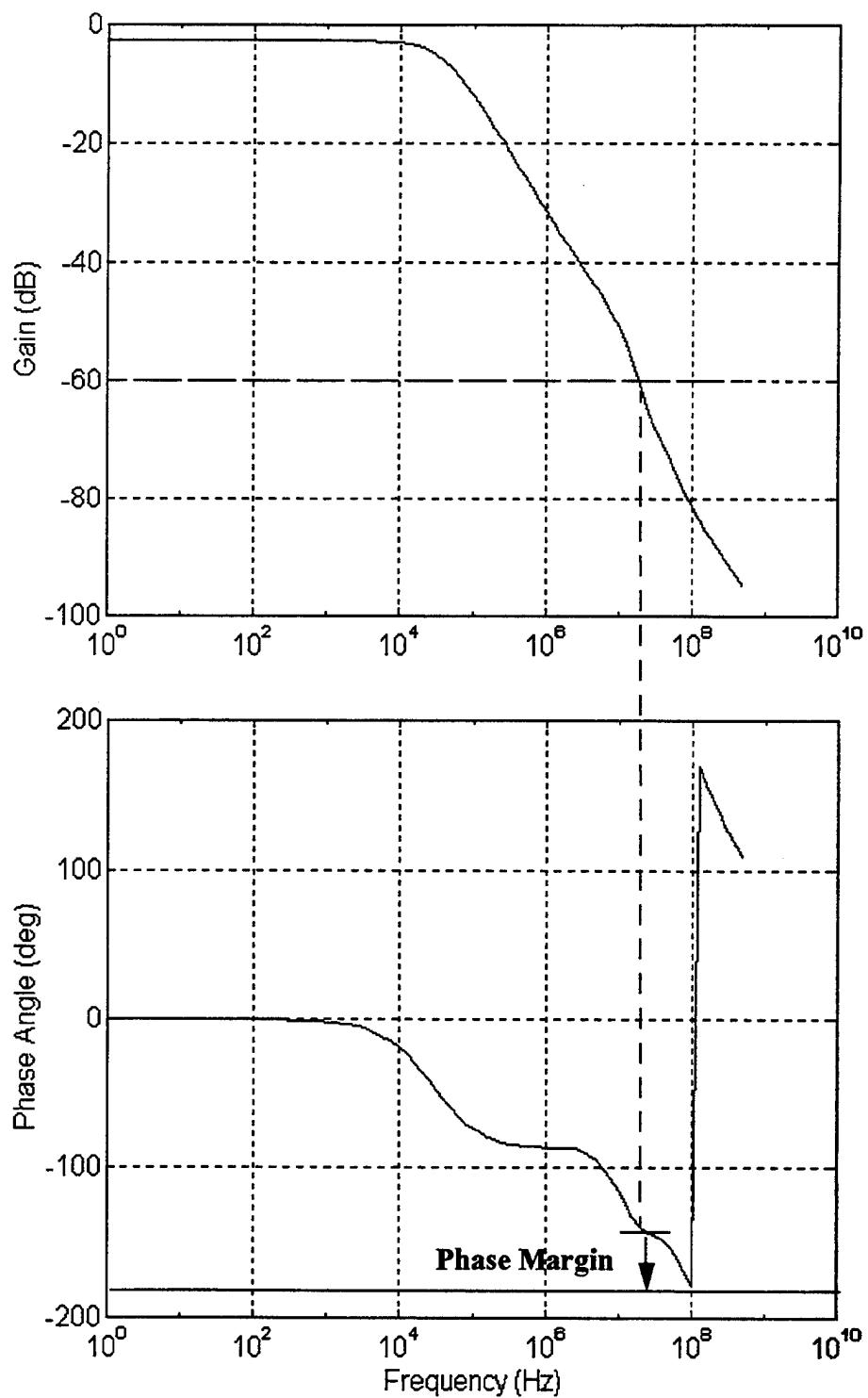
Figure 42: Composite op amp frequency response
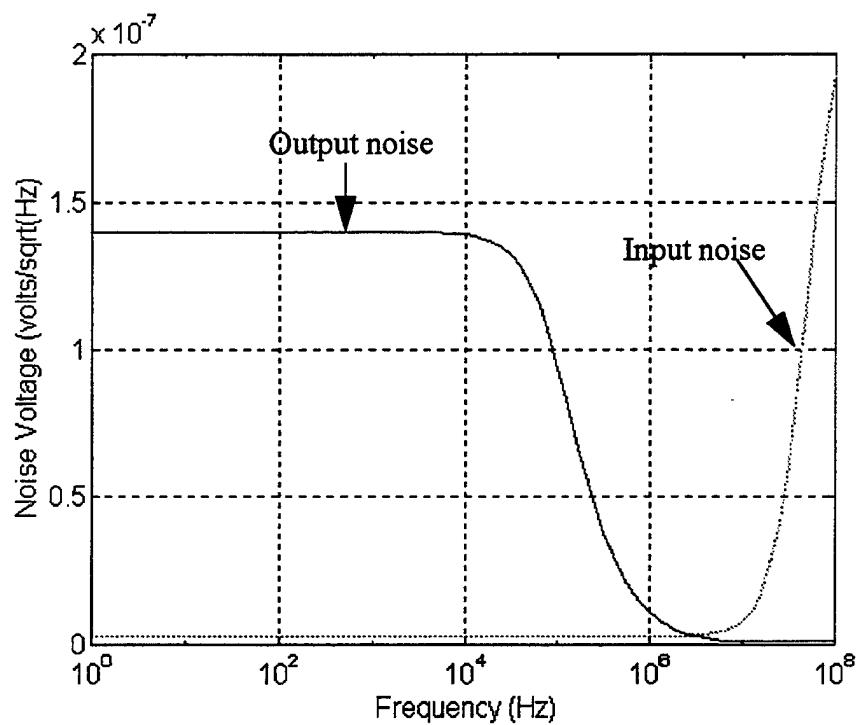
Figure 43: Noise analysis of the pseudo-BiCMOS op amp

Parameter	Holman/Connelly's CMOS LFA	Holman/Connelly's BiLNA	Improved Stability BiLNA
-3 dB frequency (@ 20 dB gain)	301 kHz	11.1 Mhz	2.24 Mhz
E_n@ 1 Hz	6.5 $nV/\sqrt{Hz}$	23.8 $nV/\sqrt{Hz}$	2.86 $nV/\sqrt{Hz}$
Phase margin	-	-90°	45°
Input bias current	-	1.68 μA	3.03 μA
Input offset current	-	14.0 nA	3.08 μA
Input offset voltage	35.4 μV	1.0 mV	511 μV
CMRR	- 141 dB	99.6 dB	59.2 dB
PSRR +	-132 dB	67.6 dB	12.4 dB
PSRR -	- 108 dB	73.9 dB	2.35 dB
Slew Rate +	2.03 $V/\mu s$	39.0 $V/\mu s$	11.2 $V/\mu s$
Slew Rate -	2.03 $V/\mu s$	42.5 $V/\mu s$	12.0 $V/\mu s$
Quiescent current	0.75 mA	2.1 mA	1.1 mA

Table 3: Summary of op amp comparisons

VII. CONCLUSIONS AND RECOMMENDATIONS

A. CONCLUSIONS

An operational amplifier using parasitic lateral bipolar transistors in CMOS was designed for fabrication. Its operation was simulated, and its low voltage capability was verified. The stability of this design over that of Holman and Connelly was demonstrated. This improvement in stablility prevented the design from achieving the gain bandwidth product of the previous design. However, the resulting gain bandwidth product of this design is still larger than that of a purely CMOS operational amplifier with equivalent topology. This design should also have a low input noise characteristics.

The area needed to build a usable lateral bipolar transistor is considerably large when compared with the area needed by a regular CMOS transistor. The lateral bipolar must be placed where it has the greatest effect. Liberal incorporation in designs will be prevented by its large size.

Though touted as a low voltage amplifier, this amplifier performs best with power supplies of ± 6 V. This is where it achieves its best open loop gain. The open loop gain varies greatly with power supply. Thus, operational amplifier is very susceptible to noise in its power supply.

Time did not allow for the fabrication and testing of the amplifier design. All conclusions are drawn by the results of the simulation alone.

B. RECOMMENDATIONS

The fabricated amplifier should be tested and compared against the simulation results presented here. This will allow for better models of the lateral bipolar transistor that is realized in the CMOS process.

The following is also recommended:

1. The amplifier should be fabricated in the best process affordable to shorten the base width of the lateral bipolar transistor. This will greatly improve its performance and the performance of the overall design as well.

2. This amplifier is a perfect candidate for use as a voltage comparator or as a component in a sample and hold circuit of an analog-to-digital converter. Applications to portable battery operated devices that have need for this circuit would be especially attractive because this amplifier could operate at very low voltages.

3. The composite amplifier configuration is an excellent way to improve the performance of this amplifier, especially if higher open loop gain and bandwidth are desired.

4. This amplifier would also be useful in a VLSI implementation of a programmable GIC filter circuit that is realized using switched capacitor technology. This circuit depends greatly on a high performance, CMOS or BiCMOS op amp.

5. Since one of the negative aspects of this amplifier was its low PSRR, more work should be dedicated to improve this problem.

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9. Pulfrey, D.L. and Torr, N.G., *Introduction to Microelectronic Devices*, Prentice Hall, Englewood Cliffs, NJ, 1989.

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11. Mikhael, W.B. and Michael, S.N., "Composite Operational Amplifiers: Generation and Finite-Gain Applications," in IEEE Transactions on Circuits and Systems, v.CAS-34, No. 5. pp. 449-460, IEEE, New York, NY, May 1987.

APPENDIX A. PSPICE SIMULATION CODE

This appendix contains the PSPICE simulation code that was used in this thesis.

A. OPEN-LOOP

```
Improved Stability BiLNA Op Amp - Open-loop
****** Model for the Lateral Bipolar ******
.MODEL QLAT LPNP (Bf=150 Br=150 VAf=16V Is=6e-17 Tf=1.807ns
+Rb=6000 Rc=4000 Re=40 Cje=1.0fF Vje=0.75V Mje=0.3333 Cjc=1fF Vjc=0.75V
+Mjc=0.3333 Cjs=3.0pF Vjs=0.52V Mjs=0.5 Itf=1 Xtf=0 Vtf=10 Tr=1n Tf=1.807n
+Ne=1.5 Ikf=14.68u Xtb=1.5 Br=1 Nc=2 Ikr=0 Eg=1.11 Fc=0.5)
****** Subcircuit for the Parasitic Lateral Bipolar
.SUBCKT PNPLAT2 1 2 3
*1 = Lateral Collector 2 = Base 3 = Emitter
VSENSE 3 4 0
Q1 1 2 4 0 QLAT 40
FVERT 1 0 VSENSE 0.45
.ENDS
****** Models for NMOS and PMOS Transistors
.MODEL nfet NMOS LEVEL=2 PHI=0.600000 TOX=4.0900E-08 XJ=0.200000U
+ VTO=0.8521 DELTA=6.0730E+00 LD=3.7400E-07 KP=4.5609E-05
+ UO=540.2 UEXP=1.7910E-01 UCRIT=1.2460E+05 RSH=1.7720E+01
+ GAMMA=1.0020 NSUB=2.1560E+16 NFS=7.2650E+12 VMAX=8.0710E+04
+ LAMBDA=2.8110E-02 CGDO=4.7365E-10 CGSO=4.7365E-10
+ CGBO=3.4581E-10 CJ=3.8438E-04 MJ=0.4448 CJSW=5.7330E-10
+ MJSW=0.315202 PB=0.800000 TPG=1
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0040E-09
.MODEL pfet PMOS LEVEL=2 PHI=0.600000 TOX=4.0900E-08 XJ=0.200000U
+ VTO=-0.8979 DELTA=2.2360E-01 LD=2.8960E-07 KP=1.9900E-05
+ UO=235.7 UEXP=2.9240E-01 UCRIT=6.5870E+04 RSH=3.5610E+01
+ GAMMA=0.6838 NSUB=1.0040E+16 NFS=8.1810E+12 VMAX=9.9990E+05
+ LAMBDA=4.8910E-02 CGDO=3.6676E-10 CGSO=3.6676E-10
+ CGBO=3.4581E-10 CJ=1.9685E-04 MJ=0.4747 CJSW=1.2242E-10
+ MJSW=0.020888 PB=0.700000 TPG=-1
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0020E-09
******* Model for Diode
.model dmod D (Is=100pA n=1.679)
```

```
******* Op Amp described as subcircuit bcopamp
.subckt bcopamp 7 6 14
X1  8 6 16   PNPLAT2
M2  8 8 17 17 nfet   L=18u  W=480u
M3  16 4 1 1 pfet   L=4u   W=1296u
X4  10 7 16  PNPLAT2
M5  10 8 17 17 nfet   L=18u  W=480U
M6  12 4 1 1 pfet   L=4u   W=512u
M7  12 10 17 17nfetL=3u   W=108u
M8  12 12 17 17 nfetL=7u   W=44u
M9  13 12 17 17nfetL=4u   W=46u
M10 13 13 1 1pfetL=4u   W=82u
M11 14 13 1 1  pfetL=2u   W=270u
M12 14 10 17 17nfetL=2u   W=384u
M13  4  2 5 17nfetL=7u   W=58u
M14  4  4 1 1 pfetL=4u   W=47u
M15  2  4 1 1 pfetL=4u   W=47u
M16  2  2 3 17 nfet  L=7u   W=58u
D1   3  17dmod
R1   5  17 22K
RZ  15 10    2K
Cc  15 14 22p
Cb  1 4     10p
* Power Supply
Vdd 1 0 DC +2.5V
Vss 17 0 DC -2.5V
.ends
****** Open loop circuit with op amp in unity gain as load
XOP1 1 2 3 bcopamp
XOP2 3 4 4 bcopamp
***** Inputs
Vin+ 1 0 AC 10mV
Vin- 2 0 DC 0
***** Analysis statements
.AC DEC 10 1Hz 100MegHz
.TRAN 0.1ns 10us
.TF V(3) Vin+
.OP
.NOISE V(3) Vin+
.print NOISE ONOISE INOISE
.probe
.end
```

B. UNITY GAIN AND SLEW RATE

```
Improved Stability BiLNA Op Amp - Unity Gain and Slew Rate
****** Model for the Lateral Bipolar ******
.MODEL QLAT LPNP (Bf=150 Br=150 VAf=16V Is=6e-17 Tf=1.807ns
+Rb=6000 Rc=4000 Re=40 Cje=1.0fF Vje=0.75V Mje=0.3333 Cjc=1fF Vjc=0.75V Fc=0.5
+Mjc=0.3333 Cjs=3.0pF Vjs=0.52V Mjs=0.5 Itf=1 Xtf=0 Vtf=10 Tr=1n Tf=1.807n
+Ne=1.5 Ikf=14.68u Xtb=1.5 Br=1 Nc=2 Ikr=0 Eg=1.11)
****** Subcircuit for the Parasitic Lateral Bipolar
.SUBCKT PNPLAT2 1 2 3
*1 = Lateral Collector 2 = Base 3 = Emitter
VSENSE 3 4 0
Q1 1 2 4 0 QLAT 40
FVERT 1 0 VSENSE 0.45
.ENDS
****** Models for NMOS and PMOS Transistors
.MODEL nfet NMOS LEVEL=2 PHI=0.600000 TOX=4.0900E-08 XJ=0.200000U TPG=1
+ VTO=0.8521 DELTA=6.0730E+00 LD=3.7400E-07 KP=4.5609E-05
+ UO=540.2 UEXP=1.7910E-01 UCRIT=1.2460E+05 RSH=1.7720E+01
+ GAMMA=1.0020 NSUB=2.1560E+16 NFS=7.2650E+12 VMAX=8.0710E+04
+ LAMBDA=2.8110E-02 CGDO=4.7365E-10 CGSO=4.7365E-10
+ CGBO=3.4581E-10 CJ=3.8438E-04 MJ=0.4448 CJSW=5.7330E-10
+ MJSW=0.315202 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0040E-09
.MODEL pfet PMOS LEVEL=2 PHI=0.600000 TOX=4.0900E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8979 DELTA=2.2360E-01 LD=2.8960E-07 KP=1.9900E-05
+ UO=235.7 UEXP=2.9240E-01 UCRIT=6.5870E+04 RSH=3.5610E+01
+ GAMMA=0.6838 NSUB=1.0040E+16 NFS=8.1810E+12 VMAX=9.9990E+05
+ LAMBDA=4.8910E-02 CGDO=3.6676E-10 CGSO=3.6676E-10
+ CGBO=3.4581E-10 CJ=1.9685E-04 MJ=0.4747 CJSW=1.2242E-10
+ MJSW=0.020888 PB=0.700000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0020E-09
******* Model for Diode
.model dmod D (Is=100pA n=1.679)
******* Op Amp described as subcircuit bcopamp
.subckt bcopamp 7 6 14
X1  8 6 16   PNPLAT2
M2  8 8 17 17 nfet   L=18u  W=480u
M3  16 4 1 1 pfet   L=4u   W=1296u
X4  10 7 16  PNPLAT2
M5  10 8 17 17 nfet   L=18u  W=480U
M6  12 4 1 1 pfet   L=4u   W=512u
```

```
M7  12 10 17 17nfetL=3u   W=108u
M8  12 12 17 17 nfetL=7u   W=44u
M9  13 12 17 17nfetL=4u   W=46u
M10 13 13 1 1pfetL=4u   W=82u
M11 14 13 1 1  pfetL=2u   W=270u
M12 14 10 17 17nfetL=2u   W=384u
M13  4 2 5 17nfetL=7u   W=58u
M14  4  4 1 1 pfetL=4u   W=47u
M15  2  4 1 1 pfetL=4u   W=47u
M16  2  2 3 17 nfet L=7u   W=58u
D1   3  17dmod
R1   5 17 22K
Rz  10 15 2K
Cc  15 14 22pF
Cb  1  4  10pF
* Power Supply
Vdd 1 0 DC +2.5V
Vss 17 0 DC -2.5V
.ends
****** Unity Gain circuit with op amp in unity gain as load
XOP1 1 3 3 bcopamp
XOP2 3 4 4 bcopamp
***** Inputs
Vin2 1 0 pulse (-1.5 1.5 1uS 0 0 5uS 10uS)
***** Analysis statements
.AC DEC 10 1Hz 100MegHz
.TRAN 0.1ns 10us
.OP
.print tran  V(3)
.probe
.end
```

C. CLOSED LOOP GAIN OF 10

```
Improved Stability BiLNA Op Amp - Closed Loop with Gain of 10
****** Model for the Lateral Bipolar ******
.MODEL QLAT LPNP (Bf=150 Br=150 VAf=16V Is=6e-17 Tf=1.807ns
+Rb=6000 Rc=4000 Re=40 Cje=1.0fF Vje=0.75V Mje=0.3333 Cjc=1fF Vjc=0.75V Fc=0.5
+Mjc=0.3333 Cjs=3.0pF Vjs=0.52V Mjs=0.5 Itf=1 Xtf=0 Vtf=10 Tr=1n Tf=1.807n
+Ne=1.5 Ikf=14.68u Xtb=1.5 Br=1 Nc=2 Ikr=0 Eg=1.11)
****** Subcircuit for the Parasitic Lateral Bipolar
.SUBCKT PNPLAT2 1 2 3
*1 = Lateral Collector 2 = Base 3 = Emitter
VSENSE 3 4 0
```

Q1 1 2 4 0 QLAT 40
FVERT 1 0 VSENSE 0.45
.ENDS
****** Models for NMOS and PMOS Transistors
.MODEL nfet NMOS LEVEL=2 PHI=0.600000 TOX=4.0900E-08 XJ=0.200000U TPG=1
+ VTO=0.8521 DELTA=6.0730E+00 LD=3.7400E-07 KP=4.5609E-05
+ UO=540.2 UEXP=1.7910E-01 UCRIT=1.2460E+05 RSH=1.7720E+01
+ GAMMA=1.0020 NSUB=2.1560E+16 NFS=7.2650E+12 VMAX=8.0710E+04
+ LAMBDA=2.8110E-02 CGDO=4.7365E-10 CGSO=4.7365E-10
+ CGBO=3.4581E-10 CJ=3.8438E-04 MJ=0.4448 CJSW=5.7330E-10
+ MJSW=0.315202 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0040E-09
.MODEL pfet PMOS LEVEL=2 PHI=0.600000 TOX=4.0900E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8979 DELTA=2.2360E-01 LD=2.8960E-07 KP=1.9900E-05
+ UO=235.7 UEXP=2.9240E-01 UCRIT=6.5870E+04 RSH=3.5610E+01
+ GAMMA=0.6838 NSUB=1.0040E+16 NFS=8.1810E+12 VMAX=9.9990E+05
+ LAMBDA=4.8910E-02 CGDO=3.6676E-10 CGSO=3.6676E-10
+ CGBO=3.4581E-10 CJ=1.9685E-04 MJ=0.4747 CJSW=1.2242E-10
+ MJSW=0.020888 PB=0.700000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0020E-09
******* Model for Diode
.model dmod D (Is=100pA n=1.679)
******* Op Amp described as subcircuit bcopamp
.subckt bcopamp 7 6 14
X1 8 6 16   PNPLAT2
M2 8 8 17 17 nfet   L=18u W=480u
M3 16 4 1 1 pfet   L=4u   W=1296u
X4 10 7 16 PNPLAT2
M5 10 8 17 17 nfet   L=18u W=480U
M6 12 4 1 1 pfet   L=4u   W=512u
M7 12 10 17 17nfetL=3u   W=108u
M8 12 12 17 17 nfetL=7u   W=44u
M9 13 12 17 17nfetL=4u   W=46u
M10 13 13 1 1pfetL=4u   W=82u
M11 14 13 1 1 pfetL=2u   W=270u
M12 14 10 17 17nfetL=2u   W=384u
M13 4 2 5 17nfetL=7u   W=58u
M14 4 4 1 1 pfetL=4u   W=47u
M15 2 4 1 1 pfetL=4u   W=47u
M16 2 2 3 17 nfet L=7u   W=58u
D1 3 17dmod

```
R1   5 17 22K
Rz   10 15 2K
Cc   15 14 22pF
Cb   1 4 10pF
* Power Supply
Vdd 1 0 DC +2.5V
Vss 17 0 DC -2.5V
.ends
****** Closed Loop Circuit with Gain of 10 with op amp in unity gain as load
XOP1 1 2 3 bcopamp
XOP2 3 4 4 bcopamp
R1 2 200 100
R2 2 3 1K
***** Inputs
Vin- 200 0 SIN (0 10mV 2.3Meg 0 0)
*Vin- 200 0 AC 10mV
VOS 1 0 dc -511uV
***** Analysis statements
*.AC DEC 10 1Hz 100MegHz
.TRAN 0.1ns 0.5us
.OP
.Print tran V(3) V(200)
.probe
.end
```

D.   HOLMAN-CONNELLY BiLNA OP AMP

```
Holman-Connelly BiLNA Op Amp
****** Model for the Lateral Bipolar ******
.MODEL QLAT LPNP (Bf=150 Br=150 VAf=16V Is=6e-17 Tf=1.807ns
+Rb=6000 Rc=4000 Re=40 Cje=1.0fF Vje=0.75V Mje=0.3333 Cjc=1fF Vjc=0.75V Fc=0.5
+Mjc=0.3333 Cjs=3.0pF Vjs=0.52V Mjs=0.5 Itf=1 Xtf=0 Vtf=10 Tr=1n Tf=1.807n
+Ne=1.5 Ikf=14.68u Xtb=1.5 Br=1 Nc=2 Ikr=0 Eg=1.11)
****** Subcircuit for the Parasitic Lateral Bipolar
.SUBCKT PNPLAT2 1 2 3
*1 = Lateral Collector 2 = Base 3 = Emitter
VSENSE 3 4 0
Q1 1 2 4 0 QLAT 40
FVERT 1 0 VSENSE 0.45
.ENDS
****** Models for NMOS and PMOS Transistors
.MODEL nfet NMOS LEVEL=2 PHI=0.600000 TOX=4.0900E-08 XJ=0.200000U TPG=1
+ VTO=0.8521 DELTA=6.0730E+00 LD=3.7400E-07 KP=4.5609E-05
+ UO=540.2 UEXP=1.7910E-01 UCRIT=1.2460E+05 RSH=1.7720E+01
```

+ GAMMA=1.0020 NSUB=2.1560E+16 NFS=7.2650E+12 VMAX=8.0710E+04
+ LAMBDA=2.8110E-02 CGDO=4.7365E-10 CGSO=4.7365E-10
+ CGBO=3.4581E-10 CJ=3.8438E-04 MJ=0.4448 CJSW=5.7330E-10
+ MJSW=0.315202 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0040E-09
.MODEL pfet PMOS LEVEL=2 PHI=0.600000 TOX=4.0900E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8979 DELTA=2.2360E-01 LD=2.8960E-07 KP=1.9900E-05
+ UO=235.7 UEXP=2.9240E-01 UCRIT=6.5870E+04 RSH=3.5610E+01
+ GAMMA=0.6838 NSUB=1.0040E+16 NFS=8.1810E+12 VMAX=9.9990E+05
+ LAMBDA=4.8910E-02 CGDO=3.6676E-10 CGSO=3.6676E-10
+ CGBO=3.4581E-10 CJ=1.9685E-04 MJ=0.4747 CJSW=1.2242E-10
+ MJSW=0.020888 PB=0.700000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0020E-09
******* Model for Diode
.model dmod D (Is=100pA n=1.679)
****** Holman-Connelly circuit
X1 8 6 16   PNPLAT2
M2 8 8 17 17 nfet   L=18u W=480u
M3 16 4 1 1 pfet   L=3.6u W=1296u
X4 10 7 16 PNPLAT2
M5 10 8 17 17 nfet   L=18u W=480U
M6 12 4 1 1 pfet   L=3.6u W=511.2u
M7 12 10 17 17nfetL=3.6u W=129.6u
M8 12 12 17 17 nfetL=6.6u W=43.8u
M9 13 12 17 17nfetL=3.6u W=45.6u
M10 13 13 1 1pfetL=3.6u W=81.6u
M11 14 13 1 1 pfetL=1.2u W=270u
M12 14 10 17 17nfetL=1.2u W=384u
M13 4 2 5 17 nfetL=7.2u W=58.2u
M14 4 4 1 1 pfetL=3.6u W=46.8u
M15 2 4 1 1 pfetL=3.6u W=46.8u
M16 2 2 3 17 nfet L=7.2u W=58.2u
D1   3 17dmod
R1   5 17 34K
Rz   10 15 300
Cc   15 14 1pF
Cb   1 4 5pF
*Power Supply
Vdd 1 0 DC +2.5V
Vss 17 0 DC -2.5V
Vin1 6 0 DC 0

Vin2 7 0 AC 10mV
****** Analysis
*.DC Vin2 -0.5 0.5 0.1V
.AC DEC 10 1Hz 100MegHz
.probe
.end

E.   COMPOSITE CONFIGURATION

Composite Op Amp made with Improved Stability BiLNA Op Amp - Open Loop
****** Model for the Lateral Bipolar ******
.MODEL QLAT LPNP (Bf=150 Br=150 VAf=16V Is=6e-17 Tf=1.807ns
+Rb=6000 Rc=4000 Re=40 Cje=1.0fF Vje=0.75V Mje=0.3333 Cjc=1fF Vjc=0.75V Fc=0.5
+Mjc=0.3333 Cjs=3.0pF Vjs=0.52V Mjs=0.5 Itf=1 Xtf=0 Vtf=10 Tr=1n Tf=1.807n
+Ne=1.5 Ikf=14.68u Xtb=1.5 Br=1 Nc=2 Ikr=0 Eg=1.11)
****** Subcircuit for the Parasitic Lateral Bipolar
.SUBCKT PNPLAT2 1 2 3
*1 = Lateral Collector 2 = Base 3 = Emitter
VSENSE 3 4 0
Q1 1 2 4 0 QLAT 40
FVERT 1 0 VSENSE 0.45
.ENDS
****** Models for NMOS and PMOS Transistors
.MODEL nfet NMOS LEVEL=2 PHI=0.600000 TOX=4.0900E-08 XJ=0.200000U TPG=1
+ VTO=0.8521 DELTA=6.0730E+00 LD=3.7400E-07 KP=4.5609E-05
+ UO=540.2 UEXP=1.7910E-01 UCRIT=1.2460E+05 RSH=1.7720E+01
+ GAMMA=1.0020 NSUB=2.1560E+16 NFS=7.2650E+12 VMAX=8.0710E+04
+ LAMBDA=2.8110E-02 CGDO=4.7365E-10 CGSO=4.7365E-10
+ CGBO=3.4581E-10 CJ=3.8438E-04 MJ=0.4448 CJSW=5.7330E-10
+ MJSW=0.315202 PB=0.800000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0040E-09
.MODEL pfet PMOS LEVEL=2 PHI=0.600000 TOX=4.0900E-08 XJ=0.200000U TPG=-1
+ VTO=-0.8979 DELTA=2.2360E-01 LD=2.8960E-07 KP=1.9900E-05
+ UO=235.7 UEXP=2.9240E-01 UCRIT=6.5870E+04 RSH=3.5610E+01
+ GAMMA=0.6838 NSUB=1.0040E+16 NFS=8.1810E+12 VMAX=9.9990E+05
+ LAMBDA=4.8910E-02 CGDO=3.6676E-10 CGSO=3.6676E-10
+ CGBO=3.4581E-10 CJ=1.9685E-04 MJ=0.4747 CJSW=1.2242E-10
+ MJSW=0.020888 PB=0.700000
* Weff = Wdrawn - Delta_W
* The suggested Delta_W is 2.0020E-09
******* Model for Diode
.model dmod D (Is=100pA n=1.679)
******* Op Amp described as subcircuit bcopamp

```
.subckt bcopamp 7 6 14
X1  8 6 16   PNPLAT2
M2  8 8 17 17 nfet   L=18u  W=480u
M3  16 4 1 1 pfet   L=4u   W=1296u
X4  10 7 16  PNPLAT2
M5  10 8 17 17 nfet   L=18u  W=480U
M6  12 4 1 1 pfet   L=4u   W=512u
M7  12 10 17 17nfetL=3u   W=108u
M8  12 12 17 17 nfetL=7u   W=44u
M9  13 12 17 17nfetL=4u   W=46u
M10 13 13 1 1pfetL=4u   W=82u
M11 14 13 1 1 pfetL=2u   W=270u
M12 14 10 17 17nfetL=2u   W=384u
M13  4 2 5 17nfetL=7u   W=58u
M14  4 4 1 1 pfetL=4u   W=47u
M15  2 4 1 1 pfetL=4u   W=47u
M16  2 2 3 17 nfet  L=7u   W=58u
D1  3  17dmod
R1  5 17 22K
Rz  10 15 2K
Cc  15 14 22pF
Cb  1 4 10pF
* Power Supply
Vdd 1 0 DC +2.5V
Vss 17 0 DC -2.5V
.ends
***** Composite Subcircuit
.subckt comopamp 1 2 5
Xa1 2 3 4 bcopamp
Xa2 1 4 5 bcopamp
Rc1 3 1 500
Rc2 3 4 100
.ends
***** Composite Op Amp in Open-Loop Configuration with load bcopamp
XOP1 1 0 3 comopamp
XOP2 3 4 4 bcopamp
***** Inputs
Vin2 1 0 AC 1mV
***** Analysis Statements
.AC DEC 10 1Hz 500MegHz
.probe
.print ac Vp(3)
.end
```

APPENDIX B. COLOR MAGIC LAYOUTS

This appendix contains color graphics of MAGIC layouts of the PNP emitter dot structure, the operational amplifier and the four amplifier pad ring.
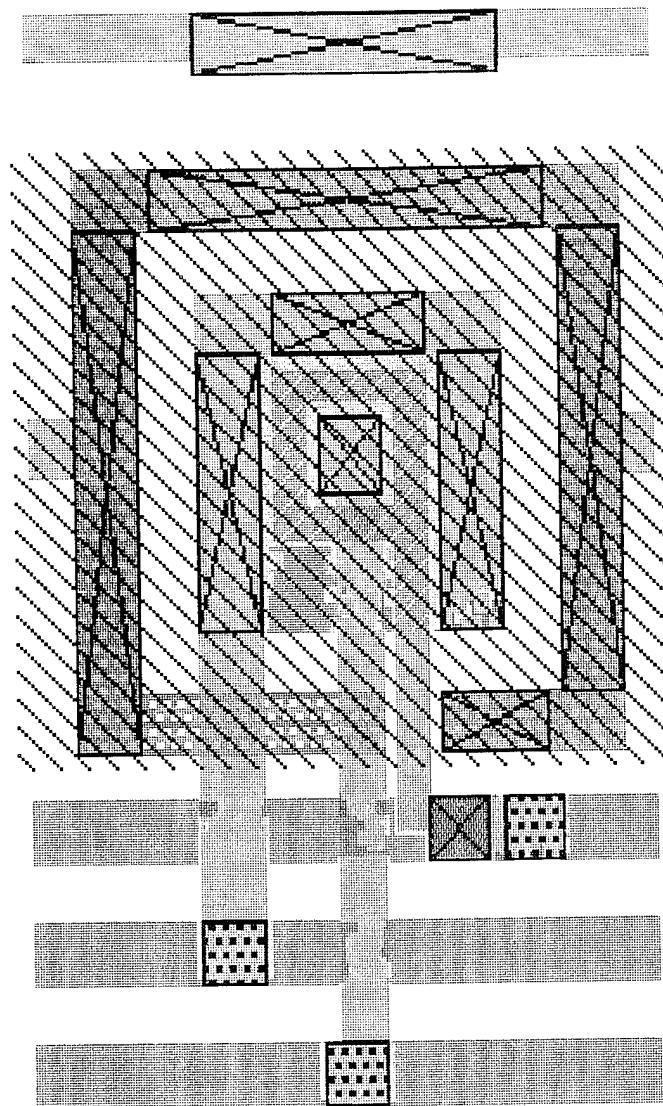
Appendix Figure 1: The emitter dot structure
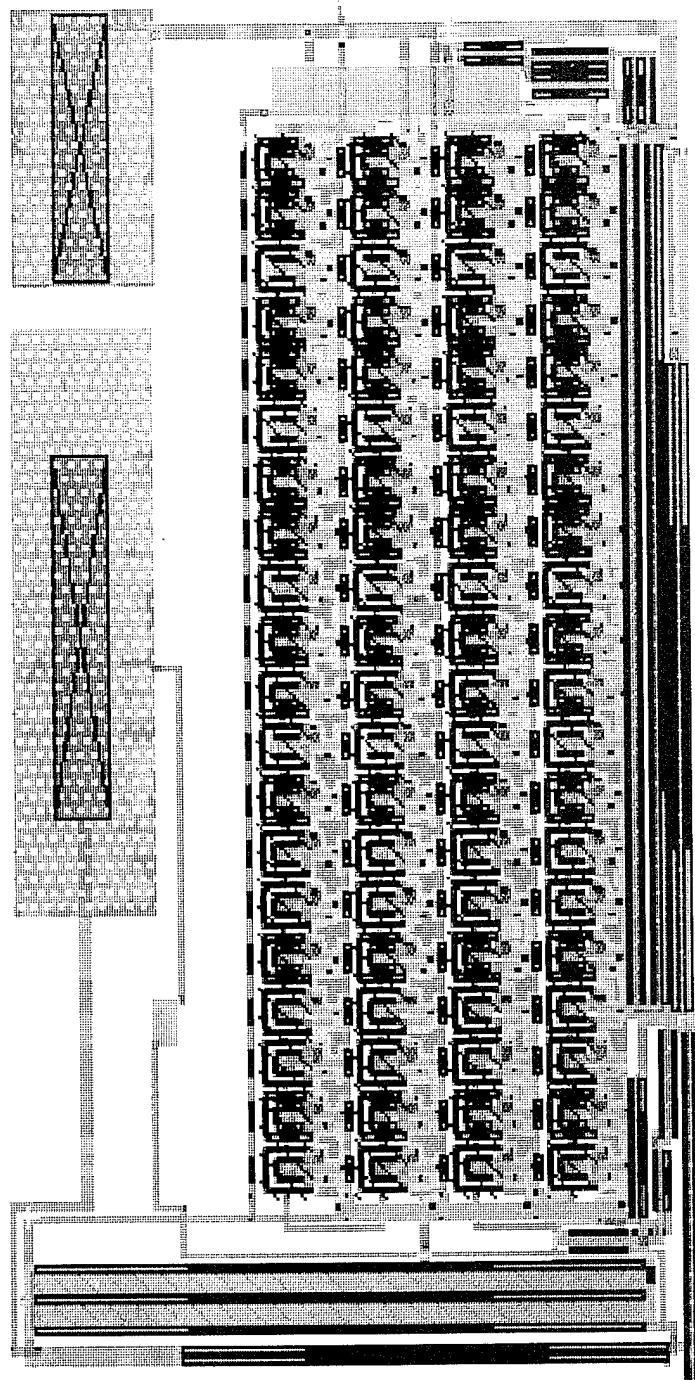
Appendix Figure 2: Magic layout of BiCMOS operational amplifier
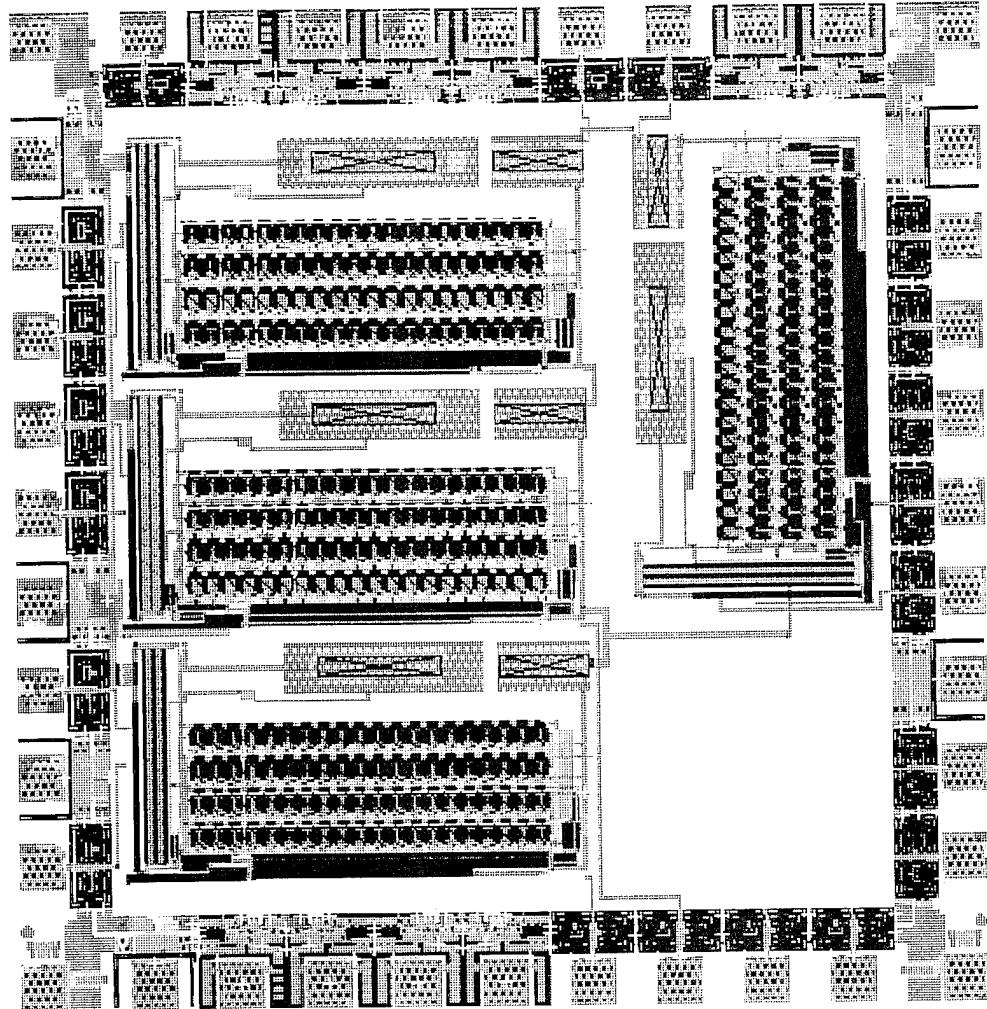
Appendix Figure 3: The four amplifier pad ring

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